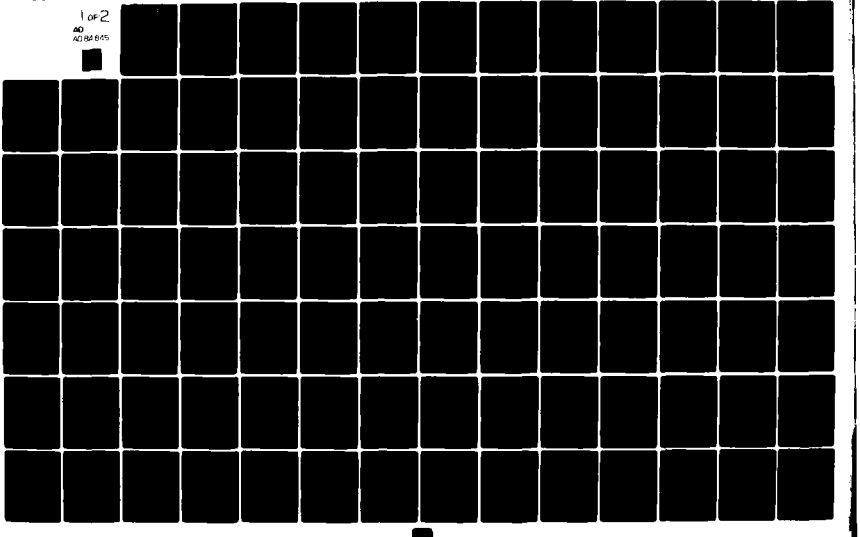
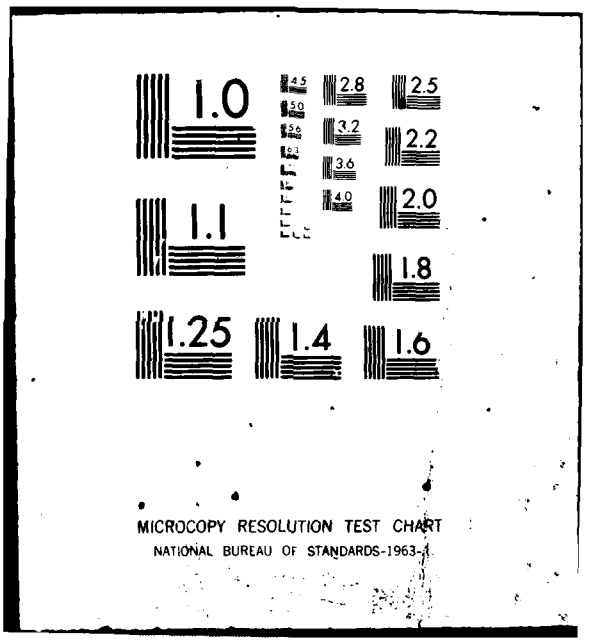
AD-A084 645 BOEING CO SEATTLE WASH F/G 9/5
A TOTAL DOSE HOMOGENEITY STUDY OF THE 108A OPERATIONAL AMPLIFIE--ETC(U)
OCT 79 A H JOHNSTON, C A LANCASTER DNA001-78-C-0216
UNCLASSIFIED DNA-4977F NL

1 OF 2
AD
AD A084 645




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

A TOTAL DOSE HOMOGENEITY STUDY OF THE 108A OPERATIONAL AMPLIFIER

The Boeing Company
P.O. Box 3999
Seattle, Washington 98124

1 October 1979

Final Report for Period 30 May 1978—1 October 1979

CONTRACT No. DNA 001-78-C-0216

THIS WORK SPONSORED BY THE DEFENSE NUCLEAR AGENCY
UNDER RDT&E RMSS CODE B323078464 Z99QAXTD04369 H2590D.

Prepared for
Director
DEFENSE NUCLEAR AGENCY
Washington, D. C. 20305

Destroy this report when it is no longer needed. Do not return to sender.

PLEASE NOTIFY THE DEFENSE NUCLEAR AGENCY, *ATTN: STTI, WASHINGTON, D.C. 20305*, IF YOUR ADDRESS IS INCORRECT, IF YOU WISH TO BE DELETED FROM THE DISTRIBUTION LIST, OR IF THE ADDRESSEE IS NO LONGER EMPLOYED BY YOUR ORGANIZATION.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER DNA 4977F	2. GOVT ACCESSION NO. AD-A084645	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* A TOTAL DOSE HOMOGENEITY STUDY OF THE 108A OPERATIONAL AMPLIFIER		5. TYPE OF REPORT & PERIOD COVERED Final Report for Period 30 May 78—1 Oct 79
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Allan H. Johnston Christy A. Lancaster		8. CONTRACT OR GRANT NUMBER(s) DNA 001-78-C-0216
9. PERFORMING ORGANIZATION NAME AND ADDRESS The Boeing Company P.O. Box 3999 Seattle, Washington 98124		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Subtask Z99QAXTD043-69
11. CONTROLLING OFFICE NAME AND ADDRESS Director Defense Nuclear Agency Washington, D.C. 20305		12. REPORT DATE 1 October 1979
		13. NUMBER OF PAGES 124
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS *(of this report)* UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

This work sponsored by the Defense Nuclear Agency under RDT&E RMSS Code B323078464 Z99QAXTD04369 H2590D.

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Total Dose
Operational Amplifier
Space Radiation Effects
Hardness Assurance
Homogeneity

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This study investigated the homogeneity of the total dose degradation of 108A-type operational amplifiers. The homogeneity was investigated at the diffusion lot, wafer and subwafer levels, using devices with individual wafer and diffusion lot traceability. The results show that relatively large differences occurred in the variability of the radiation response of devices from different diffusion lots. Much smaller differences occurred for devices from the same wafer or diffusion lot. The response variability

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

20. ABSTRACT (Continued)

of devices at the subwafer level was not much lower than that of the entire wafer unless devices were restricted to small regions of the wafer. It was also demonstrated that breakout transistors or circuits with poorer electrical specifications could be used as test patterns for the low yield 108A op-amps. A small number of devices had abnormally high or low responses which could not be reliably identified by small lot sample testing. Additional system margin must be provided to allow for this behavior.

SUMMARY

This study investigated the radiation response variability of total dose degradation of 108A-type operational amplifiers. Complete circuits and breakout transistors were obtained with wafer and diffusion lot traceability from three different diffusion lots. Two wafers were obtained with x-y coordinate traceability so that subwafer homogeneity of the radiation response could be examined.

Radiation testing was done using a mobile bias test fixture which continually applied bias to the devices during irradiation and in between irradiations. A ^{60}Co source was used for irradiation. All electrical measurements were completed within 15 minutes after irradiation. Annealing (under bias) was investigated, and input bias current recovered to approximately one-half the initial irradiated value after 1000 hours.

The homogeneity results for the three diffusion lots showed that the variability of the radiation response of devices from a single wafer was comparable to that of devices from a single diffusion lot. Examination of local variations in the radiation response at the subwafer level showed that these variations were almost as large as that of the entire wafer unless the area was confined to a very small region of the wafer, and subwafer sampling is probably not of value for low yield devices such as the 108A. Based on these results, diffusion lot traceability appears to be the optimum level for device identification and sample testing.

Test data from the 108A circuits generally agreed well with data from circuits with looser electrical specifications (i.e., 308A, 108). The degradation of breakout transistors could also be correlated with circuit degradation from the same diffusion lots. These devices, which are more abundant than the scarce 108A circuits, can be used as test samples for the 108A devices. This is extremely important for devices like the 108A, where only a small number of devices from each wafer meet the initial electrical specifications.

A small number of devices—approximately one percent of the total sample—were found to have abnormally high or low radiation responses. Attempts to correlate this behavior with pre-irradiation electrical data were unsuccessful. Additional margin must be used in systems designs to allow for such devices.

Test results for the AMD 108A devices showed that these devices work satisfactorily at levels above 10^6 rad(Si). There is some degradation, but no catastrophic failures occurred. Small sample testing was an effective way of verifying the hardness level of the three diffusion lots.

Many of the results of this study can be used as a guide in selecting hardness assurance methods for other linear devices. The information about degradation of the different types of linear transistors is particularly valuable. There are variations between manufacturing processes and internal design that must be taken into account, but those results should provide better insight into the linear circuit hardness assurance problem than the less systematic results from system users.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

SECTION 1

INTRODUCTION

1-1 GENERAL.

This report describes the results of a homogeneity study of total dose degradation of the 108A operational amplifier. The goal of the study was to investigate variations in total dose behavior at various levels of traceability so that specific recommendations could be made for testing and controlling linear circuits which must survive high total dose levels. The study was motivated by the need of hardened systems for more complete information on hardness variability before selecting hardness assurance methods and by the special problem of low yield devices, where individual wafer testing may be impractical.

For the experimental work on this program, special devices were procured that had the required diffusion lot, wafer and subwafer traceability. The homogeneity of the radiation response was determined by comparing the uniformity of the radiation damage with varying levels of traceability. The variation of initial electrical parameters was also considered in analyzing the results.

The results of this study provide information about the degradation of the unique transistor structures used in modern linear integrated circuits which is applicable to a wide variety of circuit types. This includes the dependence of total dose damage on biasing, nonlinearity of damage with fluence, and annealing over time periods of several hundred hours.

In addition, specific hardness assurance methods are discussed for linear integrated circuits, using the 108A results as an example.

1-2 UNITS OF MEASUREMENT.

Metric units are used throughout this report. Absorbed dose is commonly measured in rad (material) instead of Gray (material) as specified by current preferred metric units. Table 1 lists the conversion from conventional units to preferred metric units.

Table 1. Conversion factors for customary and standard metric units.

To Convert From	To	Multiply By
rad (material)	Gray (material)	1.000×10^{-2}

SECTION 2

BACKGROUND

2-1 TOTAL DOSE EFFECTS IN BIPOLAR DEVICES.

Total dose degradation of bipolar devices is a complex area of research that has been studied for many years, primarily using discrete transistors as a vehicle for study. Although there are no good quantitative models to describe this degradation, the basic mechanisms which cause gain loss in transistors have been identified as

1) charge accumulation within the SiO_2 layer
2) creation of interface states at the Si-SiO_2 interface
3) charge accumulation of the SiO_2 surface ("Telstar effect") caused by collection of positive ions on the surface.

The magnitude of these effects depends upon the physical construction of the device and on the processing steps used, particularly those that affect the Si-SiO_2 interface. The interface-state density following irradiation also depends on the bias conditions during irradiation (maximum reverse bias is generally a worst-case condition).

Total dose damage in transistors is usually larger at low measurement currents because the initial base current is lower, and therefore the relative effect of an increase in surface recombination current is greater at low currents. This is particularly significant for the input stages of linear circuits, which use transistors that are operated at low current densities. Although the change in h_{FE}^{-1} is often used to describe total dose damage, this parameter is usually non-linear with total dose, saturating at higher doses, and varying in magnitude between different units of the same device type. It is important to remember that Δh_{FE}^{-1} is not fundamentally related to internal mechanisms that control gain for total dose degradation (unlike neutron damage where Δh_{FE}^{-1} is expected to be linear with neutron fluence). In order to empirically characterize total dose damage, it is necessary to measure Δh_{FE}^{-1} at several doses and operating currents. The biasing conditions during irradiation must also be specified, and should approximate actual use conditions.

Because of the dependence of total dose damage on processing, better homogeneity is expected between devices from the same diffusion lot or wafer. However, there are no theoretical normalizing factors (such as t_B for neutron damage in transistors), and no procedure other than empirical testing exists for estimating the variability in total dose response at various traceability levels.

Only limited work has been done on the homogeneity of total dose effects for discrete transistors. A study done by Boeing in 1972 showed that the total dose response of wafers from the same diffusion run was not uniform, and concluded that sampling tests and traceability are necessary at the wafer level.[1] The Jet Propulsion Laboratory recently evaluated lot sample testing for discrete transistors, and also concluded that wafer level sampling was necessary for optimum hardness assurance control using lot sample testing.[2] In both of these studies, wide differences in homogeneity occurred between different device types. Because of these differences, it is not clear that wafer level traceability is sufficient for all types of devices. Furthermore, as discussed in the next section, the differences in construction between linear integrated circuits and discrete transistors limits the applicability of these results.

2-2 SPECIFIC PROBLEMS FOR LINEAR INTEGRATED CIRCUITS.

The complex design of modern operational amplifiers affects the analysis and interpretation of total dose degradation. Two factors must be considered:

1) These devices contain special internal components such as super-β NPN and lateral PNP transistors which are different in construction from conventional discrete transistors.

2) Because of the circuit design, the degradation of standard external parameters is difficult to relate to the degradation of internal transistor h_{FE}.

2-2.1 Special Transistor Structures.

In order to minimize production costs, most commercial linear designs use a process that is optimized for NPN transistors. Lateral PNP and substrate PNP transistors can be produced with this standard process. Although these PNP structures have low gain and poor frequency response, they can be used in high-performance linear circuits by using innovative circuit design. For some circuits, such as the 108A, a special high-gain NPN transistor ("super-β" transistor) is produced by adding a second emitter diffusion that further reduces the base width.

Cross-sectional drawings of the four transistor structures are shown in Figure 1. The relative vertical dimension is highly magnified compared to the horizontal dimension in this figure. Note that the active base region of the lateral PNP transistor is directly under the surface, and that the surface area of the base is very large. This makes the lateral PNP inherently quite sensitive to surface recombination. The vertical PNP base also has a large surface area, which makes it more sensitive to surface recombination than the NPN structures. The two PNP structures are expected to be inherently more sensitive to total dose than the NPN structures because of the large base surface area.

2-2.2 Linear Circuit Failure Mechanisms.

Only limited work has been done to analyze the mechanisms that cause total dose failure in operational amplifiers. Palkuti, Sivo and Greegor selectively irradiated different areas of 108-type op-amps, which experimentally established the internal region of the device causing external circuit parameters to fail.[3] Stanley and Gauthier[4] used a scanning electron microscope (SEM) irradiation to do a similar study that included empirical determination of first-stage current source and output stage failure. However, neither of these studies quantitatively related external circuit parameters to internal transistor degradation or considered the effect of variations in internal operating currents and gain margin on circuit failure. The competing failure mechanisms that are important in degradation of op-amp input stages are difficult to determine by empirical testing. Circuit analysis can be used to determine the effect of statistical variations in operating currents and gain margin and such an analysis is a necessary complement to test data.

Hand analysis techniques have been used to determine failure mechanisms for the 108A after neutron irradiation.[5] This study showed the importance of internal operating currents within the device in establishing gain margins, and demonstrated that the normal electrical requirements do not adequately control these margins. The variations in gain and gain degradation were relatively unimportant compared to the variations in degradation of internal operating currents. The degradation of internal PNP transistors was quantitatively related to changes in input offset voltage and internal bias currents, which established the important failure mechanisms. Competing failure mechanisms for first-stage bias current were identified using this approach. The results of this work can be extended to the

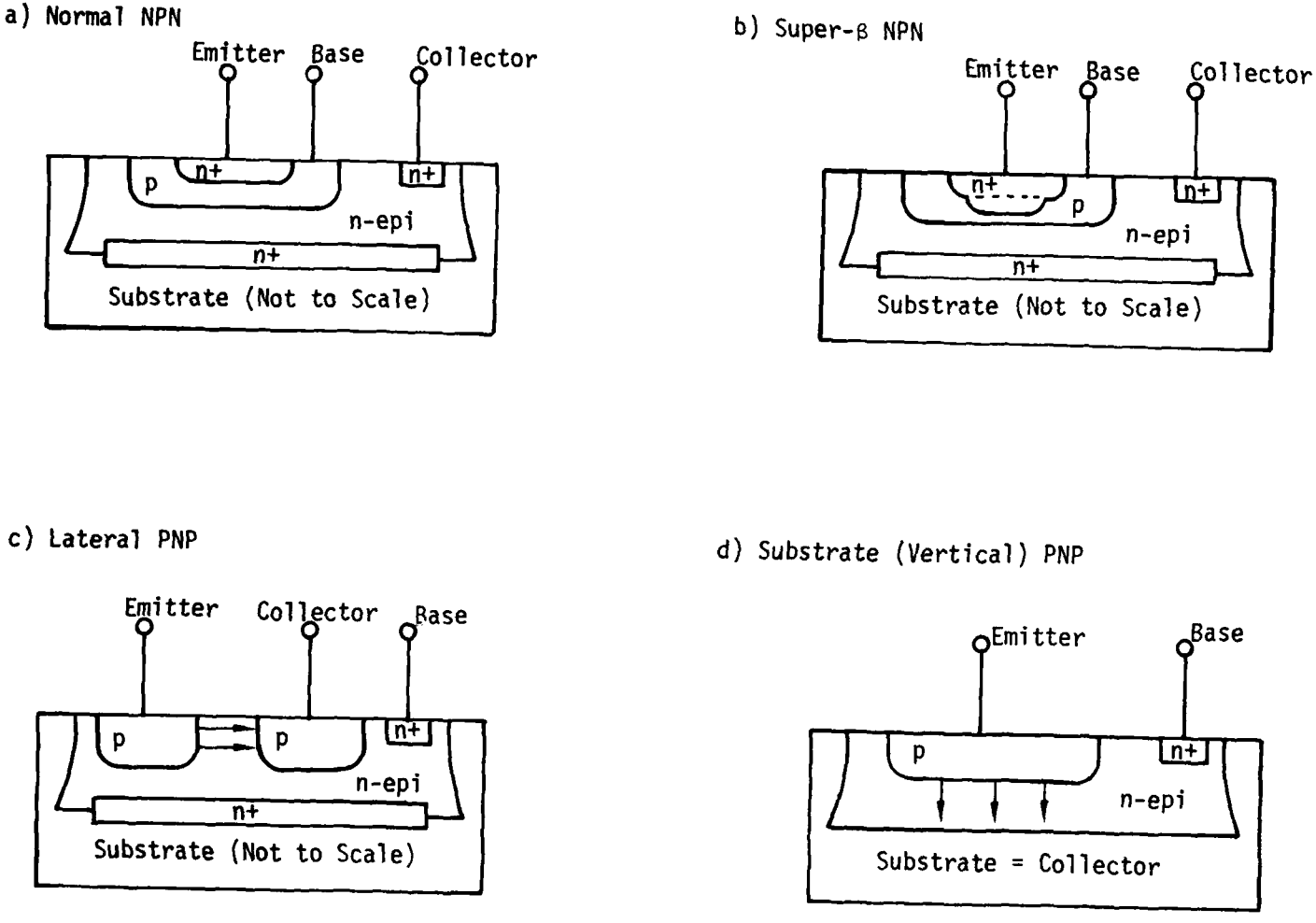


Figure 1. Cross-sections of the four transistor structures used in linear integrated circuits.

total dose environment in a straightforward manner, provided the gain degradation of component transistors is known.

An important conclusion of this study was that because of the dependence of internal bias currents on gain independent parameters (such as V_{BE} and resistor matching), the control of internal transistor degradation is not sufficient to control the behavior of complex linear circuits after irradiation. Large statistical variations occur in the internal operating currents, and these differences may dominate the statistics of the radiation behavior unless explicit controls are added to restrict their variation.

SECTION 3

TECHNICAL APPROACH

3-1 OVERALL PROGRAM DESCRIPTION.

The homogeneity study was based on 108A type op-amps from three different diffusion lots, produced by one vendor. Complete circuits and breakout transistors were procured that had wafer and diffusion lot traceability; in addition, two wafers had x-y coordinate traceability so that subwafer homogeneity could be examined.

After delivery by the manufacturer, initial electrical tests were made on all devices. Initial exploratory tests were made on the breakout transistors to characterize the fluence dependence (linearity) of the damage, investigate the dependence of damage on bias conditions during irradiation, and determine the effect of different irradiation time periods on damage. After these exploratory tests, devices from each wafer were tested with low-injection operating conditions which approximated the operating conditions within the actual integrated circuit.

The circuits from each wafer were also tested to determine the homogeneity at various traceability levels. These data were compared with the breakout transistor results from the same wafers, and the failure mechanisms for the different types of parametric failures were determined by analysis. A special circuit experiment was also completed to examine annealing of circuit parameters over a 1000 hour time period.

With the exception of the constant irradiation period experiment, all devices were irradiated under bias in a Gammacell 220 ^{60}Co irradiation cell. A mobile bias fixture was used to apply bias during irradiation and to allow devices to be transported under bias to the measuring instruments. All irradiation and measurement procedures were fully compliant with Military Specification Method 1019 for total dose irradiation. Further details are described in Section 9 of this document.

3-2 PARTS FABRICATION AND TRACEABILITY.

3-2.1 Wafer Fabrication.

All devices used in this study were fabricated by Advanced Micro Devices (AMD), Sunnyvale, California, using their standard commercial wafer fabrication process. AMD was selected because their standard process is much harder than that

of other manufacturers,[3] and many space systems use their devices because of superior radiation tolerance. Their 108A is produced on 5.08 centimeter (2 inch) diameter wafers which contain approximately 1000 die. In addition, there are three rows of test transistor patterns that were used to provide special breakout transistors from each wafer.

Devices were selected from three different diffusion lots, as shown in the overall fabrication flow of Figure 2. Wafer and diffusion lot traceability was maintained for all devices throughout the fabrication, assembly and testing. In addition, x-y coordinate traceability was maintained for both circuits and breakout transistors for two of the eight wafers. This required serialization of individual die prior to scribing and assembly. Maintaining this serialization is a major problem in a standard high-reliability assembly line.

3-2.2 Testing and Assembly.

The wafers were initially probe tested to 108A specifications. This identified potentially good die at the wafer stage. Probe testing is limited to room temperature, and the yield of 108A die is much lower when tested over the complete temperature range. However, complete temperature testing can only be done after packaging. There was no way to ascertain that acceptable yields of 108A devices would be achieved after packaging from wafer probe measurements alone, so some risk was involved with this approach. Before scribing and dicing, photographs of each wafer were taken which showed the location of 108A die at the wafer stage. For the two x-y wafers, these photographs also included individual die locations.

The wafers were then scribed and broken, taking care to retain wafer identity, and, for the two x-y wafers, individual die locations. At this point, breakout transistors were separated from the circuits because they were not subjected to burn-in or visual inspection. The individual die were then attached to headers, bonded, and subjected to visual inspection. Visual inspection criteria for surface metallization scratches were relaxed; this increased the yield without affecting the radiation hardness. After capping, a colored dot system was used to identify wafers, and the serial numbers of x-y die were scribed on the package. All circuits were then burned in using the standard 125°C, 168 hour burn-in procedure.

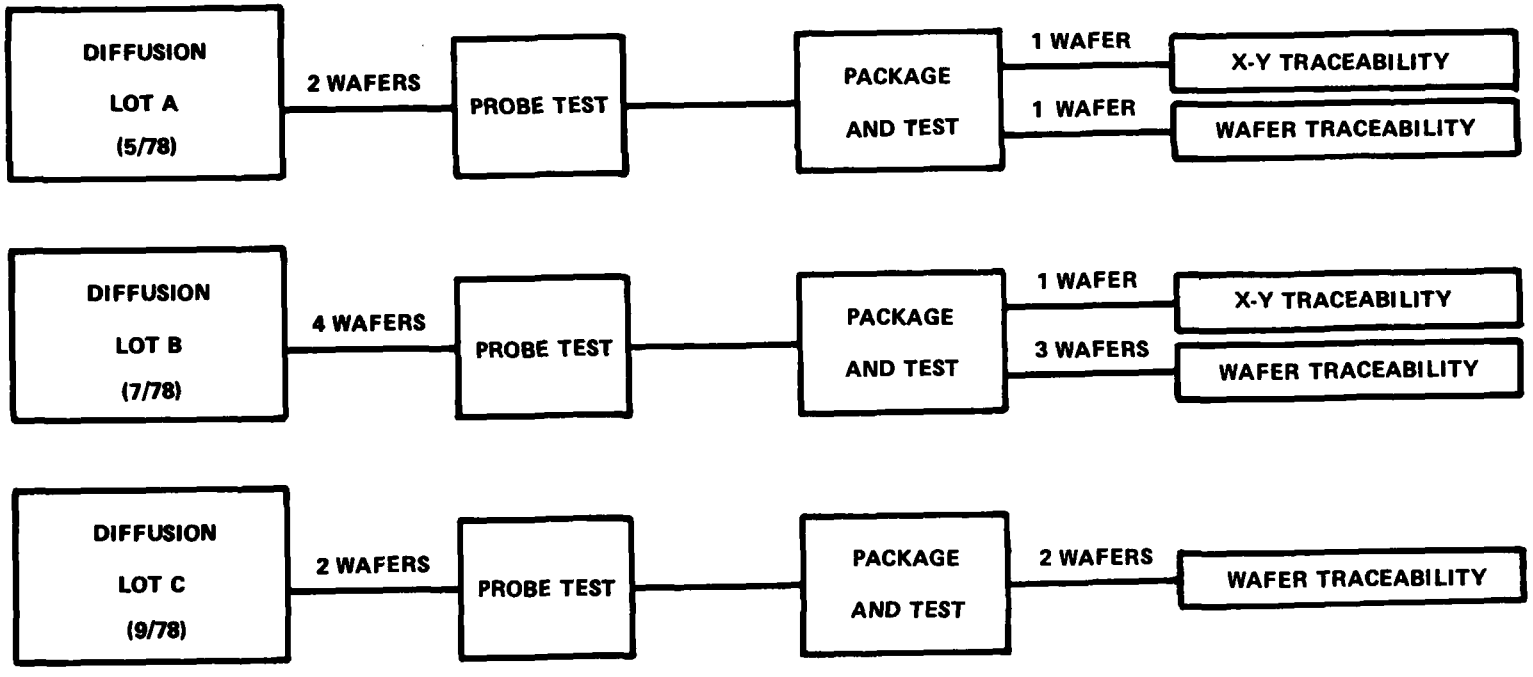


Figure 2. Diagram of device fabrication and production flow.

After burn-in, devices were tested at -55°C, 25°C and 125°C and categorized as 108A, 108, 308A, 308 or reject devices. The electrical specifications of these various part classifications are listed in Table 2.

Table 2. Electrical specifications of the 108A-type op-amps.

Device Type	Parameter Limit (Room Temperature)				
	V_{OS} (mV)	I_B (nA)	I_{OS} (nA)	A_{OL}	I_{CC} (mA)
108A	0.5	2.0	0.2	80K	0.6
308A	0.5	7.0	1.0	80K	0.8
108	2.0	2.0	0.2	50K	0.6
308	7.5	7.0	1.0	50K	0.8

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

I_{OS} = Input Offset Current

A_{OL} = Open-Loop Gain (loaded with 10K load resistance)

I_{CC} = Power Supply Current

A summary of the various wafers is listed in Table 3 below. In order to protect the interest of AMD, no specific yield information is included in this document.

Table 3. Wafer history for devices in the homogeneity study.

Diffusion Lot	Processing Start Date	Wafer No.	Comments	Radiation Hardness
A	5-7-78	71		Intermediate Hardness
		76	x-y Traceability	
B	7-11-78	2	x-y Traceability	Hardest Diffusion Lot
		5		
		6		
		16		
C	9-12-78	3		Most Sensitive Diffusion Lot
		14		

3-2.3 Acknowledgment.

This program could not have been accomplished without the cooperation of AMD. There are extreme difficulties in implementing wafer and x-y traceability on a standard production line because the normal production procedure requires complex documentation and control methods which are intended to prevent deviation from standard assembly techniques. The special marking and lot identification can only be maintained by careful coordination at each step of the assembly process. The authors wish to express their appreciation to Advanced Micro Devices and in particular to Jim Townsend, who coordinated their activity and solved the difficult practical problems of maintaining the required traceability on a commercial fabrication line.

SECTION 4

BREAKOUT TRANSISTOR EXPERIMENTS

4-1 INTRODUCTION.

The purposes of the breakout transistors were to provide more basic information about the internal properties of the integrated circuit structure, to assist in determining failure mechanisms, and to investigate the linearity of damage for internal transistors. The transistors provide better information about the bias dependence and linearity of radiation damage than the complete circuit. This is particularly important because three of the four transistor structures used in the 108A are sufficiently different from discrete transistors that it is difficult to estimate their radiation behavior from existing data on conventional discrete transistors.

All four types of transistors were available in test patterns on AMD 108-type wafers, but the physical limitation of bonding and packaging made it impossible to obtain a single package which contained all transistor types. Therefore, two different bonding patterns were used, which resulted in the two types of test patterns listed in Table 4. Two different NPN geometries were included, the small area device used in internal circuitry and the large area output geometry. The geometry of the lateral PNP was that of the second-stage transistors; the gain of these transistors strongly affects the input offset voltage. The super-β transistor geometry was the same as that of the input transistors. The only available substrate transistor geometry was the very large output transistor geometry. This transistor has an emitter area which is approximately seven times greater than that of the internal substrate transistor used in the first-stage biasing circuitry. For comparison the geometries of several other transistors which are important in various circuit failure modes are also listed in Table 4.

4-2 ELECTRICAL CHARACTERISTICS.

The electrical characteristics of the four breakout transistor types are of interest, particularly for the unique transistor structure used in linear circuits. Typical electrical parameters for the breakout transistors are listed in Table 5. The super-β NPN transistors have extremely high initial gains, which are required in order to meet the input bias current specification of the circuit. The extremely low breakdown voltage is due to the high gain. The gain of the two PNP

Table 4. Transistors available in A1 and A3 bonding patterns.

Bonding Pattern	*Transistor Designation	Description	Emitter Area [cm^2]	108A Circuit Application
A1	Q_x	Standard NPN	3.48×10^{-5}	Standard NPN Transistor
	Q_{10}	Lateral PNP	6.67×10^{-5}	Second-Stage Transistor
	Q_{19}	Vertical (Substrate) PNP	3.1×10^{-4}	Output Circuit
A3	Q_2	Super-β NPN	1.08×10^{-5}	Input Transistor
	Q_{18}	Large Area NPN	6.04×10^{-5}	Output Circuit
	Q_{19}	Vertical (Substrate) PNP	3.1×10^{-4}	Output Circuit
—	Q_{28}	Vertical (Substrate) PNP	5.43×10^{-5}	First-Stage Current Source
—	Q_{21}	Standard NPN	3.48×10^{-5}	Second-Stage Load
—	Q_{12}	Lateral PNP (Split Collector)	1.3×10^{-4}	Current Mirror

*See Figure 7 in Section 5.

Table 5. Typical electrical parameters of the breakout transistors.

Transistor Type	V_{CE} [V]	h_{FE} at $\lvert I_C \rvert$*				BV_{CEO} [V]
		10 μA	100 μA	1 mA	10 mA	
NPN (Small Geometry)	10	224	248	261	247	65
Super-β NPN	2	2090	2160	2170	-	6
Lateral PNP	-10	69.3	61.0	12.2	-	-55
Substrate PNP	-10	122	158	160	71	-90

*The sign of I_C is positive for NPN devices and negative for PNP devices.

transistors decreases rapidly with collector current, as shown for the typical devices in Figure 3. The lateral PNP transistors are only used at low currents (10-50 μA), but the output substrate PNP is required to sink up to 2 mA when the circuit is loaded, so that it must operate significantly above the peak of the h_{FE} - I_C curve.

From the standpoint of circuit operation, many of the 108A electrical parameters are more affected by V_{BE} matching of transistors and resistor ratios. Several of the breakout transistors had excessive leakage currents which affected V_{BE} at the low currents (~10 μA). These abnormalities would affect the internal bias currents of a 108A circuit, and would adversely affect the circuit operation at high temperature. They may also cause unusual radiation failure mechanisms in 108A circuits. The breakout transistors were not burned in, and were only tested at a single current by the manufacturer. Nevertheless, abnormalities in their electrical behavior provide information about the causes of circuit-to-circuit variations in electrical behavior of the 108A circuits.

Approximately 15 units of each bonding pattern (see Table 4) were obtained from each wafer. Table 6 contains a summary of the electrical abnormalities that occurred. These can be divided into four categories: high leakage current, low breakdown voltage, shorted devices, and open-circuit devices. From the standpoint of circuit operation, the most serious problem is leakage current, particularly in the super-β transistors. High leakage current will affect the V_{BE} matching characteristics and change the ratio of the internal current sources. These leakage currents may introduce new failure mechanisms, which would cause circuits with leaky internal transistors to respond differently to radiation.

Transistors with low breakdown voltage may also introduce new failure mechanisms, provided that the breakdown voltage is near the applied voltage in the circuit. Devices with lower avalanche voltages, such as those listed in Table 6, would cause the circuit to fail electrical specifications. Transistors with shorted or open circuit conditions would, in general, cause the circuit to fail electrical specifications and would not introduce new radiation failure mechanisms.

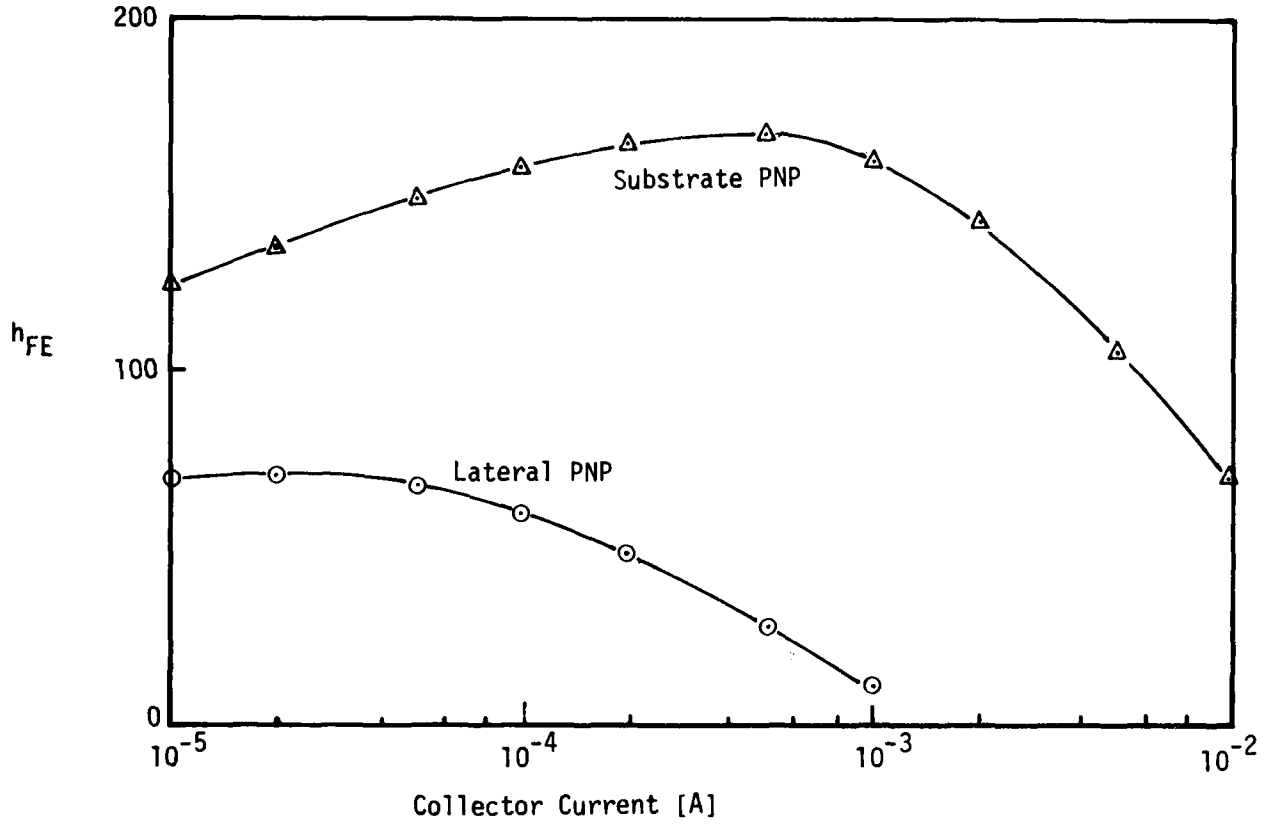


Figure 3. Typical pre-irradiation gain for lateral and substrate PNP transistors.

Table 6. Summary of electrical abnormalities of breakout transistors.

Diffusion Lot	Wafer	Transistor Type	Total	Number of Abnormal Units [Value]			
				High Leakage Current	Low Breakdown Voltage	Short	Open
A	71	NPN	2			1	1
		Substrate PNP	2		1 [7.6 V]	1	
		Lateral PNP	1				1
	76	NPN	2			1	1
		Substrate PNP	2			2	
		Lateral PNP	1				1
		Super-β NPN	2	1 [26 mA]			1
B	2	NPN	3				3
		Substrate PNP	3				3
		Lateral PNP	2				2
		Super-β NPN	1				1
	5	NPN	1				1
		Substrate PNP	3		1 [8.2 V]		2
		Lateral PNP	1				1
		Super-β NPN	1				1
	6	NPN	1				1
		Substrate PNP	3	1 [13 mA]	1 [7.4 V]	1	
		Super-β NPN	3	2 [0.3 mA, 0.36 mA]		1	
	16	NPN	2	1 [9 mA]			1
		Substrate PNP	4	1 [1.2 mA*]	2 [8.4 V, 6.8 V]		2
		Super-β NPN	1	1 [1.0 mA]		1	
C	3	Substrate PNP	1		1 [7.4 V]		
		Lateral PNP	1				1
	14	NPN	2		1 [6.8 V]		1
		Substrate PNP	1		1 [7.6 V]		
		Lateral PNP	3			1	2
		Super-β NPN	1	1 [22 μA]			

*This device also had low breakdown voltage.

4-3 BIAS DEPENDENCE OF TOTAL DOSE DAMAGE.

Total dose effects are usually worst in transistors that are reverse-biased during radiation. However, the main purpose of the test transistors was to determine the relative damage of internal transistors in an operating circuit so that the circuit failure modes could be determined. These transistors are forward-biased within the circuit during normal operation (except the overload protection transistors in the output stage). A preliminary experiment was performed with reverse-biased and forward-biased devices to compare the relative total dose damage for the two different bias conditions. The forward bias conditions approximated the biasing of internal transistors in 108A circuits.

As expected, maximum damage occurred in the reverse-biased case. There were differences in both the slope and the magnitude of Δh_{FE}^{-1} for the two bias conditions, as shown in Figure 4. Furthermore, these differences were not consistent between diffusion lots. The data in Figure 4 for the super-β transistor show a factor of four difference in Δh_{FE}^{-1} for the two wafers in the forward-biased case, whereas for the reverse-biased condition, the response of the two wafers was nearly identical.

It was apparent from these data that differences in the total dose hardness of devices within an operating circuit would not be accurately characterized by performing reverse-biased experiments on the breakout transistors. Therefore, it was decided that homogeneity comparisons should be based on forward-biased experiments on the breakout transistors, using operating currents and voltages that approximated those of the internal circuit transistors during normal operation.

4-4 DAMAGE LINEARITY AND HOMOGENEITY.

4-4.1 Damage Linearity.

The form of the dependence of transistor damage on total dose is extremely important in system applications. A quantitative description of this dependence is needed in order to apply data to systems with different radiation levels. It is also needed to determine system margin and to compare lot sample test results for hardness assurance. For this study, a quantitative description of damage is needed in order to compare the radiation hardness of different wafers and traceability levels. It is also needed to analyze the behavior of the 108A circuit.

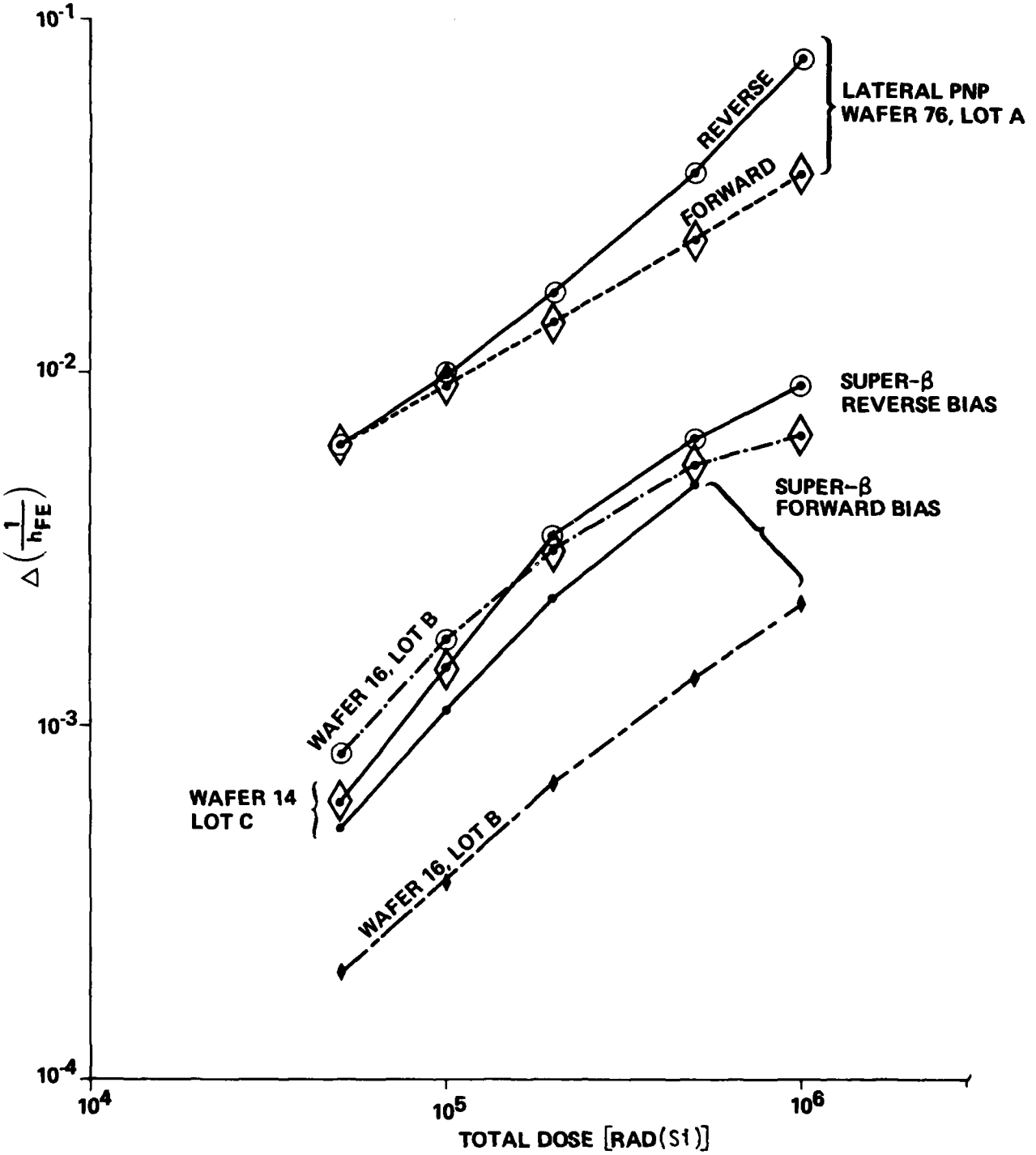


Figure 4. Delta h_{FE}^{-1} under forward and reverse bias conditions during irradiation.

As previously discussed in Section 2-1, total dose damage is usually not linear with fluence and there are no adequate models to describe the damage quantitatively. The form of the damage dependence on total dose is usually determined empirically.

Typical dependence of Δh_{FE}^{-1} on total dose for the four types of breakout transistors are shown in the log-log plots of Figure 5. The data for three of these transistor types fit a straight line with slope less than one (sublinear dependence), and can be quantitatively described by a D^N dependence, where D is the total dose. For the substrate transistor, the damage is strongly nonlinear, saturating at approximately 500 Krad(Si). This behavior is more difficult to describe quantitatively. However, the saturation of Δh_{FE}^{-1} occurs at levels well below the level at which most 108A circuits exhibit serious degradation. Differences in the saturated value of Δh_{FE}^{-1} are very important from the standpoint of circuit parameter degradation, but the exact form of the Δh_{FE}^{-1} - D relation is relatively unimportant because of the saturation. The damage factor concept is not appropriate for this saturated behavior.

The fluence dependence of the three transistors which exhibit sublinear dependence can be fitted to the equation

$$\Delta h_{FE}^{-1} = C' D^N \tag{1}$$

where N is the slope of the log-log plot and C' is a fitted proportionality constant. Examining the data, substantial differences in N occur between different devices, so that large differences in the coefficient C' occur even for devices with comparable values of Δh_{FE}^{-1}. Because it is difficult to multiply C' and D^N without computational aids, C' is difficult to interpret even though C' and N adequately characterize the damage dependence.

A more easily interpreted approach consists of first finding the slope N in equation 1 using a least-squares fit. The effective damage factor at the lowest fluence is then calculated according to

$$C_{F1} = \frac{\Delta\left(\frac{1}{h_{FE}}\right)}{D_1} = \frac{C' D_1^N}{D_1}. \tag{2}$$

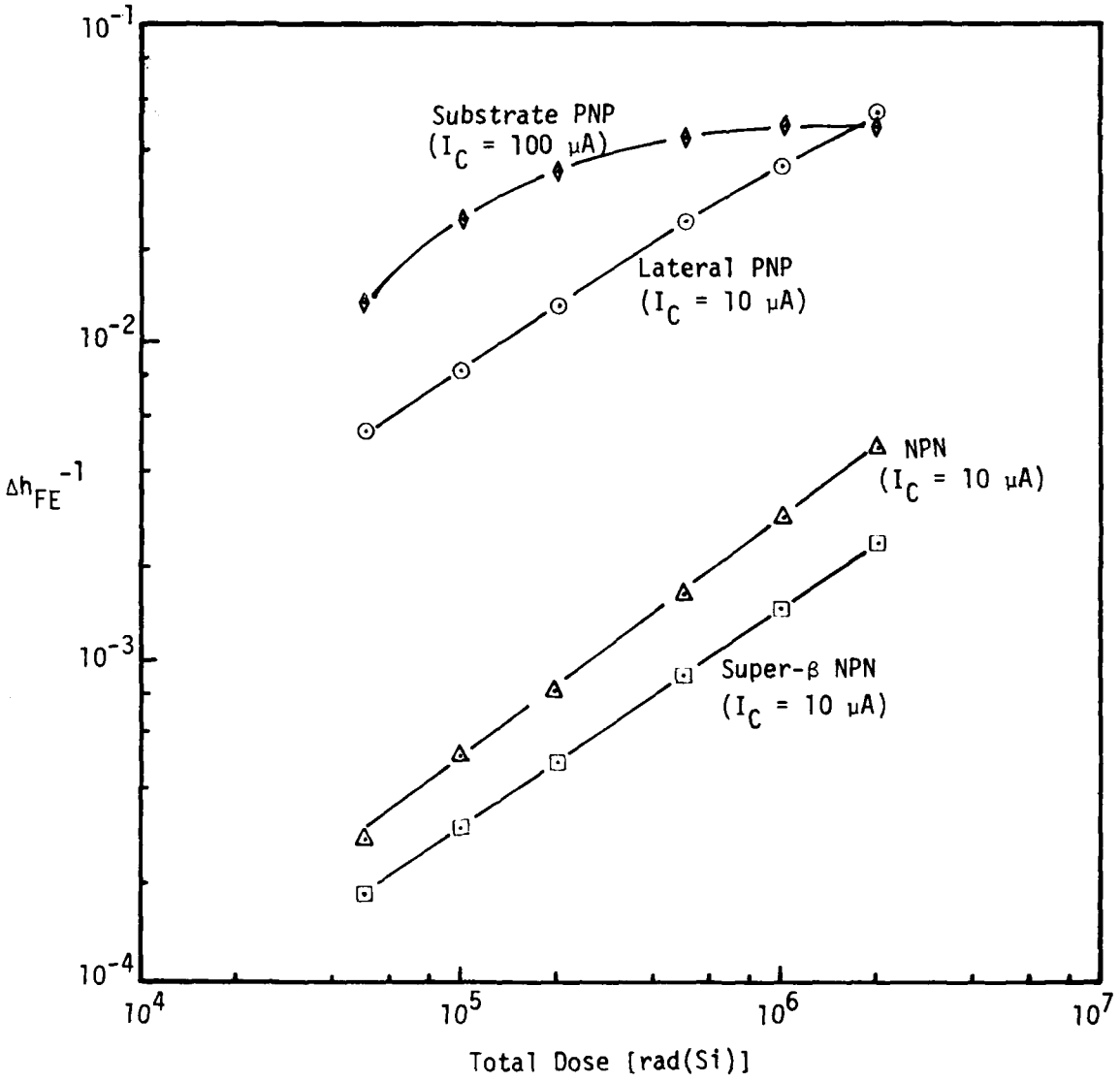


Figure 5. Comparison of damage linearity for the four types of breakout transistor components.

Although the actual data at D_1 could be used to obtain a damage factor, the least squares fit yields a coefficient that can be used to calculate Δh_{FE}^{-1} at all fluences. In most cases, C_{F1} differs from the actual damage factor at D_1 by less than 5 percent. The C_{F1} values directly compare the damage of different transistors at the lowest fluence. Above this level, the damage is sublinear with slope N and can be calculated from the equation

$$\Delta h_{FE}^{-1} = C_{F1} D_1^{(1-N)} D^N \quad (3)$$

where D_1 is the lowest fluence [5×10^4 rad(Si)].

The reason for using the fitted damage factor at D_1 to compare damage is that devices from a single wafer usually were closely matched at this level. The slopes varied substantially, even for devices from the same wafer, which caused larger variations in Δh_{FE}^{-1} at higher fluences.

4-4.2 Damage Homogeneity.

The empirical model used to characterize transistor damage in the previous section was used to compare the homogeneity of damage between the different wafers and diffusion lots. Although electrical data were taken at several different currents, the damage comparison was made only at I_C = 10 μA which approximately corresponds to the currents of the NPN, super-β and lateral PNP transistors as they are used within the 108A circuits. The total dose damage is greatest for low currents, so that this is also a "worst case" condition. As discussed in Section 4-3, all devices were forward biased during irradiation.

A summary of the total dose damage results for devices from the eight wafers is shown in Table 7 using the effective damage factor and slope defined in equation 2. The coefficient of variation (COV) is defined by the equation

$$COV = \frac{\sigma}{\bar{x}} \quad (4)$$

where σ is the standard deviation and $\bar{x}$ is the mean value of the parameter in question. The sample size for data in this table was approximately 12* units per wafer for the two wafers with x-y traceability, and six units per wafer for the other wafers. The subwafer homogeneity for the x-y wafers is discussed in Section 7.

*For the x-y traceability wafers, 11 units were irradiated from wafer 76 and 13 units from wafer 2.

Table 7. Fitted damage parameters for transistors from the eight wafers.

Wafer	Diffusion Lot	Super-β NPN				NPN				Lateral PNP			
		$\overline{C_{F1}}$	COV	$\overline{N}$	COV	$\overline{C_{F1}}$	COV	$\overline{N}$	COV	$\overline{C_{F1}}$	COV	$\overline{N}$	COV
71	A	3.98×10^{-9}	0.12	0.70	0.03	6.6×10^{-9}	0.23	0.67	0.08	1.12×10^{-7}	0.03	0.62	0.01
76*	A	4.82×10^{-9}	0.39	0.70	0.18	1.26×10^{-8}	0.06	0.62	0.04	1.23×10^{-7}	0.02	0.65	0.01
2*	B	4.95×10^{-9}	0.38	0.75	0.12	9.8×10^{-9}	0.09	0.68	0.01	1.16×10^{-7}	0.07	0.69	0.02
5	B	3.51×10^{-9}	0.18	0.86	0.11	1.22×10^{-8}	0.20	0.69	0.07	1.65×10^{-7}	0.07	0.62	0.03
6	B	4.06×10^{-9}	0.12	0.76	0.03	1.28×10^{-8}	0.12	0.64	0.04	1.21×10^{-7}	0.21	0.68	0.06
16	B	3.90×10^{-9}	0.24	0.78	0.02	6.02×10^{-9}	0.15	0.73	0.04	1.03×10^{-7}	0.07	0.66	0.02
3	C	9.25×10^{-9}	0.11	0.81	0.02	2.17×10^{-8}	0.04	0.88	0.06	1.48×10^{-7}	0.10	0.72	0.02
14	C	8.84×10^{-9}	0.14	0.85	0.02	1.94×10^{-8}	0.22	0.88	0.05	1.71×10^{-7}	0.09	0.73	0.02

*Devices from these two wafers had x-y position traceability.

Examining these data, all three types of transistors from diffusion lot C were much more sensitive to total dose than the devices from the other two diffusion lots. Not only were the mean values of C_{F1} higher, but the slopes of the h_{FE}^{-1} dependence on total dose were also larger. This causes Δh_{FE}^{-1} at high fluences to be even larger which is the region where the 108A circuits are most likely to fail. Figure 6 shows the variability in measured damage factors at 2×10^6 rad(Si), and clearly shows the increased sensitivity of the transistors from lot C. (The measured damage factor is defined in equation 1.)

Within a diffusion lot, the damage factors are more tightly grouped, but there are still substantial differences. Again, meaningful comparisons can only be made by considering both C_{F1} and N. For example, diffusion lots A and B both have one wafer with lower C_{F1} values for the NPN transistor. However, these two wafers both have higher slopes, which reduces the difference in damage factor at the higher levels near the circuit failure threshold.

The variability of damage factors within a diffusion lot must also be examined. The range of data in Figure 6 corresponds to ± 1 standard deviation and shows that the behavior of devices within a wafer is relatively uniform. Based on the data, one can conclude that diffusion lot traceability is the optimum control level for hardness assurance.

The response of the substrate transistor must also be considered. Table 8 lists the mean and coefficient of variation of Δh_{FE}^{-1} for the substrate transistors and clearly shows the saturation at higher fluence levels. The coefficient of variation is relatively low for devices from a single wafer after saturation so that the gain is relatively uniform at saturation. The saturated values of Δh_{FE}^{-1} range from approximately 0.04 to 0.08, which correspond to gains of 20 and 12, respectively.

The damage models and homogeneity results discussed in this section describe linear circuit components that are fabricated with the current AMD process for the 108A op-amp. There were substantial differences between the different diffusion lots even though they were all fabricated with the same baseline process. Although the response of transistors from a single wafer was more uniform, there were still significant differences in the slopes of the h_{FE}^{-1} dependence. The physical reason for this variation is not understood, and more work needs to be done to investigate the mechanisms of the fluence dependence.

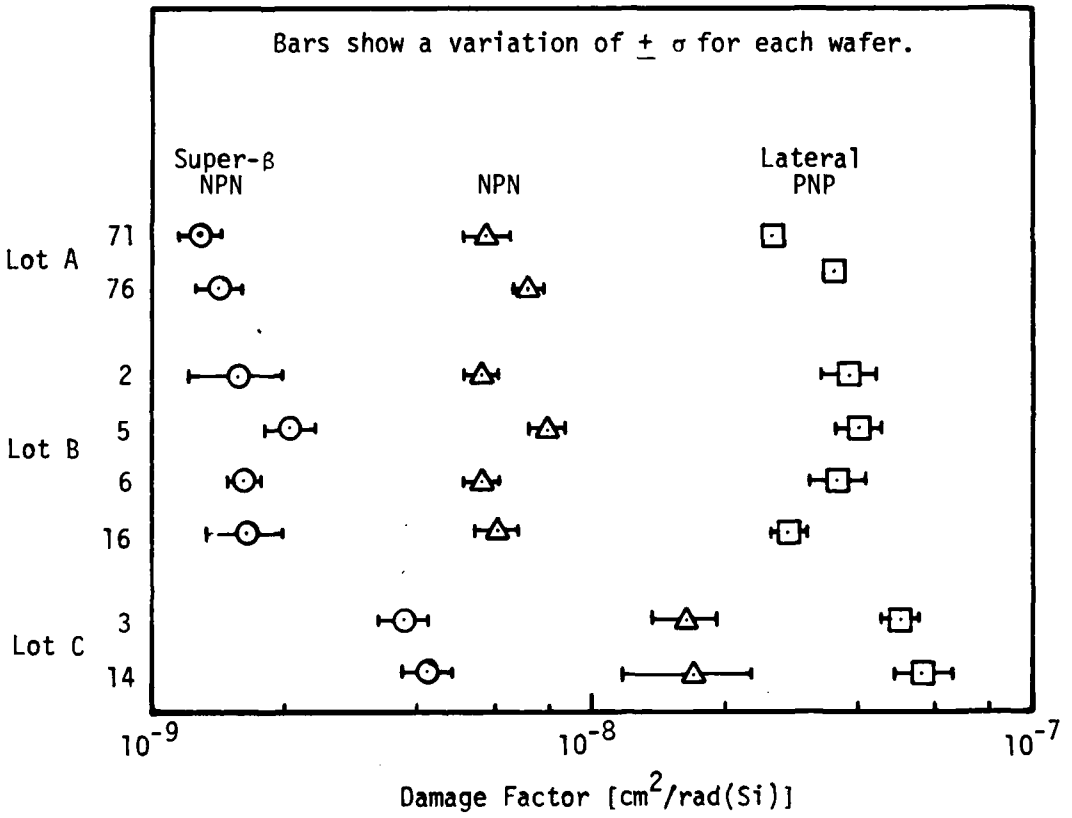


Figure 6. Breakout transistor damage factors at 2 x 10^6 rad(Si).

Table 8. Δh_{FE}^{-1} for substrate transistors.

Diffusion Lot	Wafer No.	Δh_{FE}^{-1} After Total Dose Exposure [rad(Si)]					
		5×10^4		1×10^6		2×10^6	
		Mean	COV	Mean	COV	Mean	COV
A	71	4.61×10^{-3}	0.12	3.76×10^{-2}	0.06	4.12×10^{-2}	0.07
	76	4.36×10^{-3}	0.02	3.68×10^{-2}	0.04	3.85×10^{-2}	0.05
B	2	8.97×10^{-3}	0.30	5.84×10^{-2}	0.14	6.17×10^{-2}	0.14
	5	8.48×10^{-3}	0.23	5.58×10^{-2}	0.19	5.90×10^{-2}	0.18
	6	6.95×10^{-3}	0.25	5.26×10^{-2}	0.12	5.84×10^{-2}	0.11
	16	6.47×10^{-3}	0.47	3.67×10^{-2}	0.20	4.00×10^{-2}	0.18
C	3	7.56×10^{-3}	0.19	6.44×10^{-2}	0.06	7.34×10^{-2}	0.06
	14	6.29×10^{-3}	0.06	6.82×10^{-2}	0.04	7.89×10^{-2}	0.04

SECTION 5

ANALYSIS OF THE 108A RADIATION RESPONSE

5-1 ELECTRICAL OPERATION.

Before analyzing the radiation response of the 108A op-amp it is necessary to understand its electrical operation. Discussions of the electrical and radiation response will frequently reference the electrical schematic in Figure 7. The normal NPN transistors in this figure are shown with a rectangular base symbol, while the super-β NPN devices have a conventional single line at the base. Vertical PNP transistors have their collectors routed directly to the negative supply; all other PNP structures are lateral PNP transistors.

The circuit can be analyzed more conveniently by referring to the simplified schematic of Figure 8 which eliminates the details of the various current sources. First, consider the voltage gain. The first-stage of the 108A provides high input impedance by using super-β transistors Q_1 and Q_2 at the input. The nominal value of the current source I_1 is 6 μA, and the voltage gain of the first stage is only 2.3. Essentially all of the gain is provided by the second stage, which consists of lateral PNP transistors Q_9 and Q_{10}. In order to achieve a typical gain of 100 dB or more in a single stage, extremely high load impedances are required. For $I_E \approx 6$ μA, which is the typical value of 1/2 I_2, the required load impedance is approximately 10^7 ohms. The current source loads Q_{21} and Q_{22} are interconnected to provide an extremely high effective load impedance. The voltage gain of the circuit is critically dependent on the load impedance.

The output stage consists of a complementary emitter follower connection, Q_{18} and Q_{19}. This is driven by emitter follower Q_{14}, which buffers the output stage from the current source loads of the second stage. Note that a substrate PNP transistor is used in the lower section of the output stage.

The various current sources in the 108A are important in its operation. Returning to the complete schematic of Figure 7, a reference current is established by Q_{23}, a field effect transistor (JFET). The close V_{BE} matching of transistors Q_{26} and Q_{29} is used along with resistor ratios to establish the first-stage current source I_1, which is critically important to the input parameters of the circuit. Because of the importance of V_{BE} matching, I_1 is strongly affected by leakage currents in any of the current source transistors.

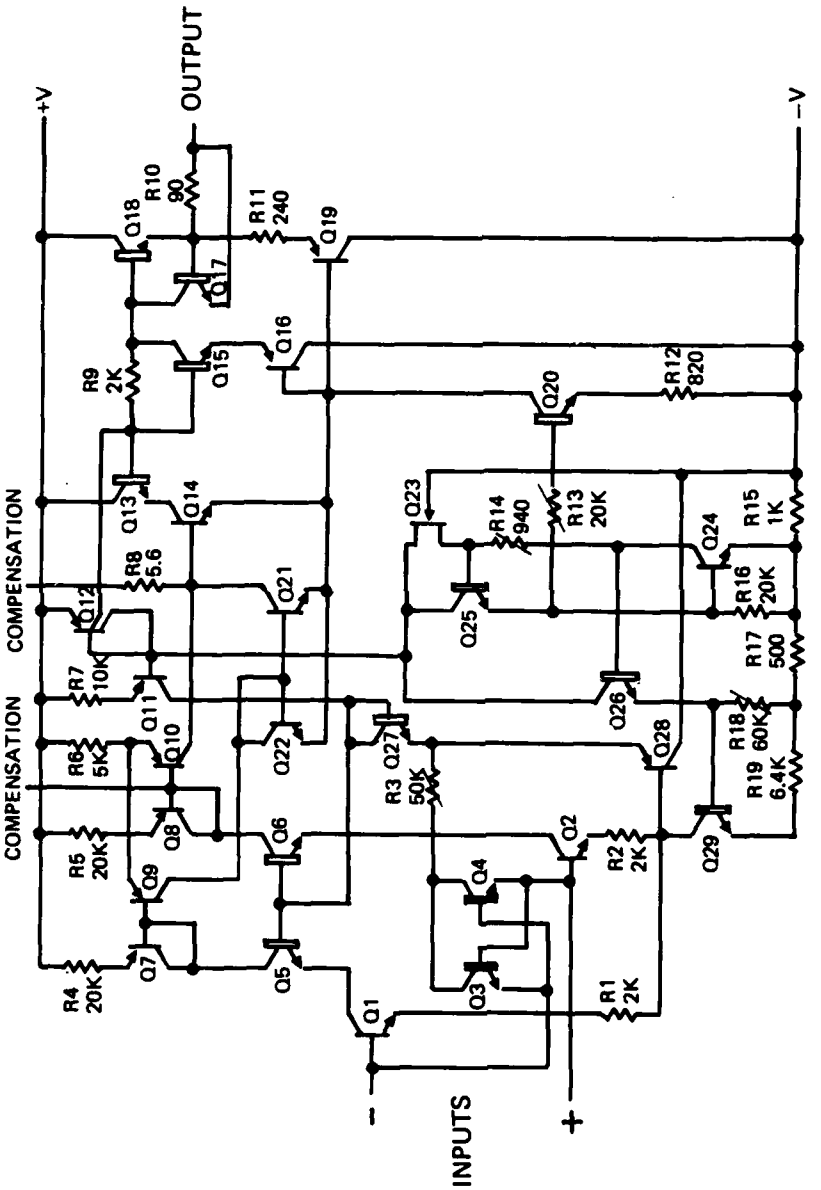


Figure 7. Complete schematic of the LM-108.

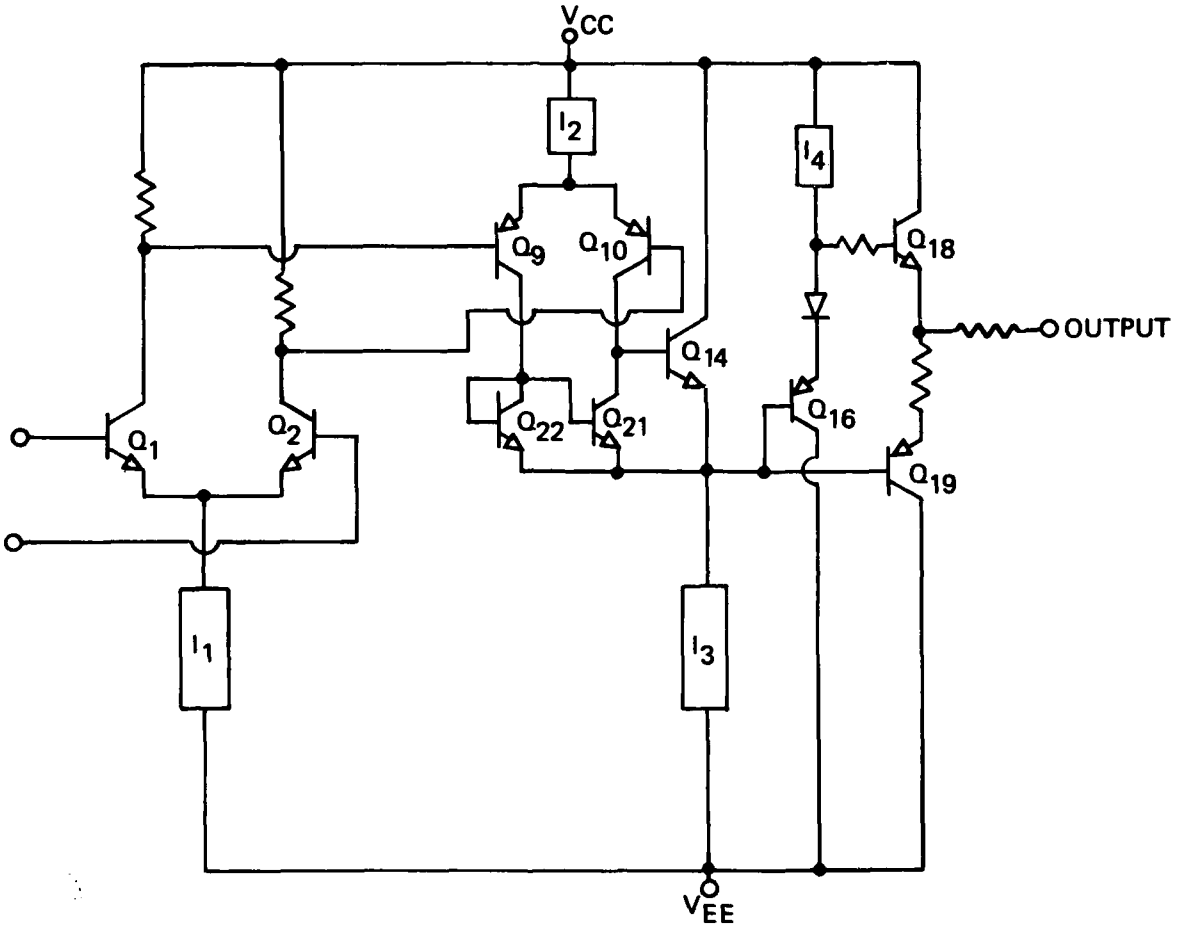


Figure 8. Simplified schematic used for analysis of the LM-108 operational amplifier.

The net current in the first-stage transistors is also affected by substrate transistor Q_{28}; its base current substracts from the current I_1. Initially this is not a problem, but it is an important failure mechanism after the substrate transistor degrades. The coupling between the first and second stages occurs through the lateral PNP transistors in the first stage. The second stage current depends on the common-base gain (α) of these transistors, and is nominally $2\alpha I_1$ because of the resistor ratios.

5-2 RADIATION FAILURE MODES.

The potential failure modes of the 108A op-amp can be analyzed as a function of the gain of internal transistors that are critical in establishing the particular failure mode. It should be emphasized that not all of these failure modes occur for the AMD version of the 108A as currently fabricated, but may be important for 108A devices from other vendors. The relative hardness of the different transistor structures is extremely important in determining the particular failure modes. In addition, nonlinearities or saturation of internal transistor damage may affect the failure modes. The failure modes for various electrical parameters will be discussed in detail in the following paragraphs.

The convention below will be used to describe the gain of the various transistor types:

1 = normal NPN transistor (e.g., h_{FE1})
2 = super-β NPN transistor
3 = lateral PNP transistor
4 = substrate PNP transistor

The pre- and post-irradiation values will be described by (0) and (D) subscripts respectively (e.g., $h_{FE1(0)}$, $h_{FE1(D)}$), and differences between two parameters after irradiation will be denoted by the prefix Δ.

5-2.1 First-Stage Current (I_1).

A reference current (I_D) within the 108A amplifier is established by the JFET, Q_{23}. Assuming matched V_{BE} characteristics for the transistors, a numerical calculation leads to the following relation for the first-stage current I_1[5]

$$I_1 = I_D \left(\frac{1}{5} - \frac{\alpha_3}{2h_{FE4}} \right) \tag{5}$$

where α_3 is the common-base gain of the current mirror transistor, Q_{12}. Assuming that the JFET current is unchanged by total dose, this current is then affected by the gain of the two PNP transistor types. In deriving this equation it is assumed that resistor ratios are constant, and the V_{BE}-I_C characteristics of the four transistors in the current source circuitry are well matched.

5-2.2 Input Bias and Input Offset Currents.

The input currents are strongly affected by the gain of the input super-β transistors and can be described by the equation

$$\frac{I_{B(D)}}{I_{1(D)}} - \frac{I_{B(0)}}{I_{1(0)}} = \Delta h_{FE2}^{-1} \tag{6}$$

where I_B is the input bias current and I_1 is the current of the internal first stage current source. This current source decreases significantly with increasing fluence, and reduces the relative change in the input bias current. Note that devices that have large decreases in I_1 will appear to be far harder to radiation, assuming equal damage factors. It can be very misleading to compare devices on the basis of ΔI_B data without also considering the effect of I_1.

Input offset current is the difference between the bias currents of the two input transistors. This parameter depends on the mismatch in the gain of the two input transistors. In most cases, the total dose behavior of the input transistors is nearly identical, and the relative change in input offset current closely corresponds to that of input bias current.

5-2.3 Input Offset Voltage.

Because of the low voltage gain of the first stage, the second stage of the 108A op-amp is equally important in determining the input offset voltage. The input super-β transistors have lower damage factors than the lateral PNP transistors in the second stage. The lateral PNP transistors are loaded differently because of the transition from differential to single-ended operation at the second stage output. The difference in loading of the second stage current sources is the dominant source of radiation-induced offset changes in the 108A. The input offset voltage of the second stage is described by the equation[5]

$$V_{OS} = \frac{kT}{q} \ln \frac{I_1 \alpha_3 \left(1 + \frac{1}{h_{FE2}}\right)}{I_1 \alpha_3 + \frac{I_{CC}}{3h_{FE2}}} \tag{7}$$

where I_1 is the bias current of the first stage, h_{FE2} is the common-emitter current gain of the super-β transistors which are current loads for the second stage, α_3 is the common-base current gain of the lateral PNP transistors, and I_{CC} is the power supply current. The super-β gain (h_{FE2}) is the most important parameter in this equation.

5-2.4 Open-Loop Gain.

A simplified expression for open-loop gain is difficult to obtain. As discussed in Section 5-1, the gain of the 108A is essentially that of the second stage and depends on matched current source loads, Q_{22}, Q_{21} and Q_{14} (these are all super-β transistors). The gain will decrease when the two current loads are no longer closely matched. The gain is affected by output load conditions because of thermal feedback within the circuit and the change in the current of buffer transistor Q_{14}. Gain degradation was relatively unimportant for the AMD devices because of the relative hardness of the substrate PNP. By the time the gain dropped to 50K, input offset voltage and input bias current were more than an order of magnitude beyond their specifications.

5-2.5 Output Drive Current.

The output drive current depends on the gain of the NPN output transistor when the amplifier operates as a current source, and on the substrate PNP output transistor when the amplifier operates as a current sink. For neutron damage, the sink current degradation is a major problem because of the sensitivity of the wide base PNP. However, the gain of this transistor saturates for the AMD 108A so that it remains well above the minimum required gain. This mechanism could be important for devices from other manufacturers.

5-2.6 Slew Rate.

The slew rate is affected by the capacitance between the two compensation leads. An external compensation capacitor is used for the 108A, with a minimum value of 30 pF. The maximum current that can charge this capacitor when the amplifier is overdriven is I_1, the first-stage current source. Slew rate degradation tracks the degradation of I_1 exactly, within experimental error.

SECTION 6

COMPARISON OF WAFER AND DIFFUSION LOT HOMOGENEITY

6-1 COMPARISON OF MEAN RESPONSES.

The most important failure mechanisms were those associated with the input parameters. The parameters V_{OS}, I_B, and I_I showed the largest changes with radiation. Slew rate degradation followed the degradation of I_I, as expected. None of the devices failed the open-loop gain specifications until the input parameters were well beyond acceptable limits, and the output sink current failure mode was not important for any of the devices. This is due to the saturation of the substrate transistor gain; the output transistor gain never falls below the minimum gain required at maximum loading.

The mean responses of these three parameters as a function of total dose are plotted in Figures 9 through 11. In each case, lot C is far more susceptible to radiation damage than the other two diffusion lots. The difference in hardness is greater than that observed for the component transistor results discussed in Section 4. This occurs because the dependence of these circuit parameters on internal transistor h_{FE} is not a simple linear dependence, and also because several different internal transistors contribute to the response mechanisms, as discussed in Section 5.

Within a single diffusion lot, relatively small differences in the radiation response were observed, which is consistent with the results of the breakout transistors. Although the possibility of a single wafer with an abnormal response cannot be ruled out, these data suggest that diffusion lot sampling is the optimum level for hardness assurance lot sampling.

Representative data at several radiation levels for circuits from each of the eight wafers are contained in Appendix A.

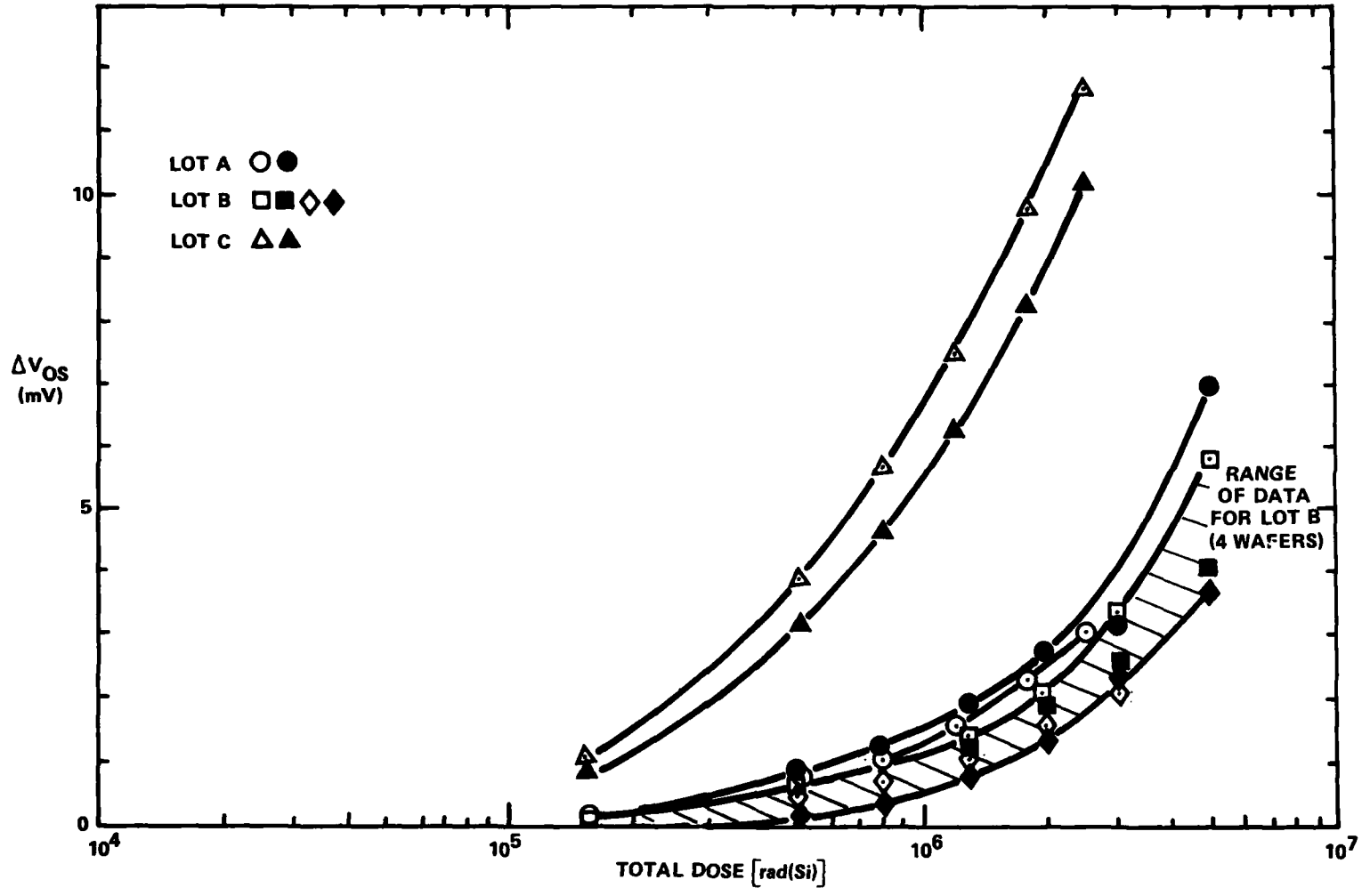


Figure 9. Change in input offset voltage with total dose.

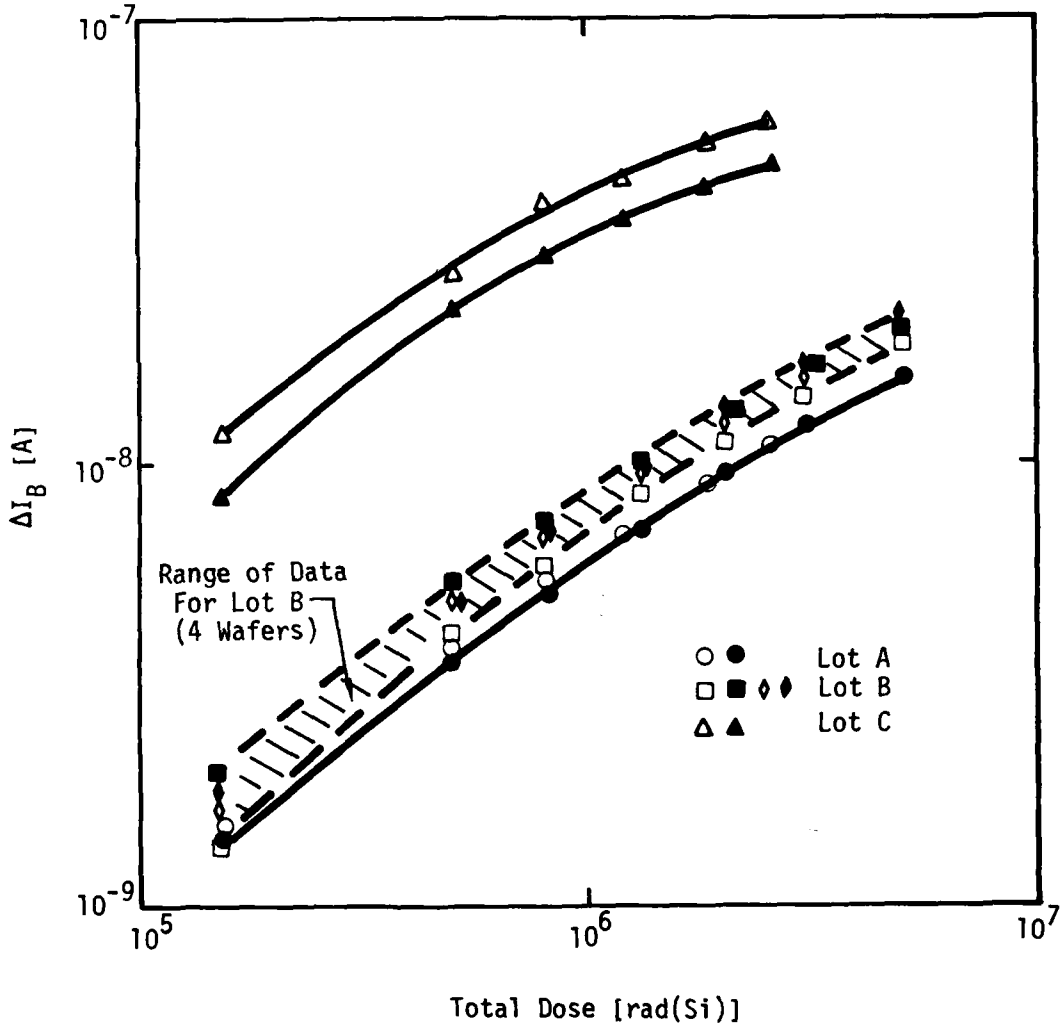


Figure 10. Change in input bias current with total dose.

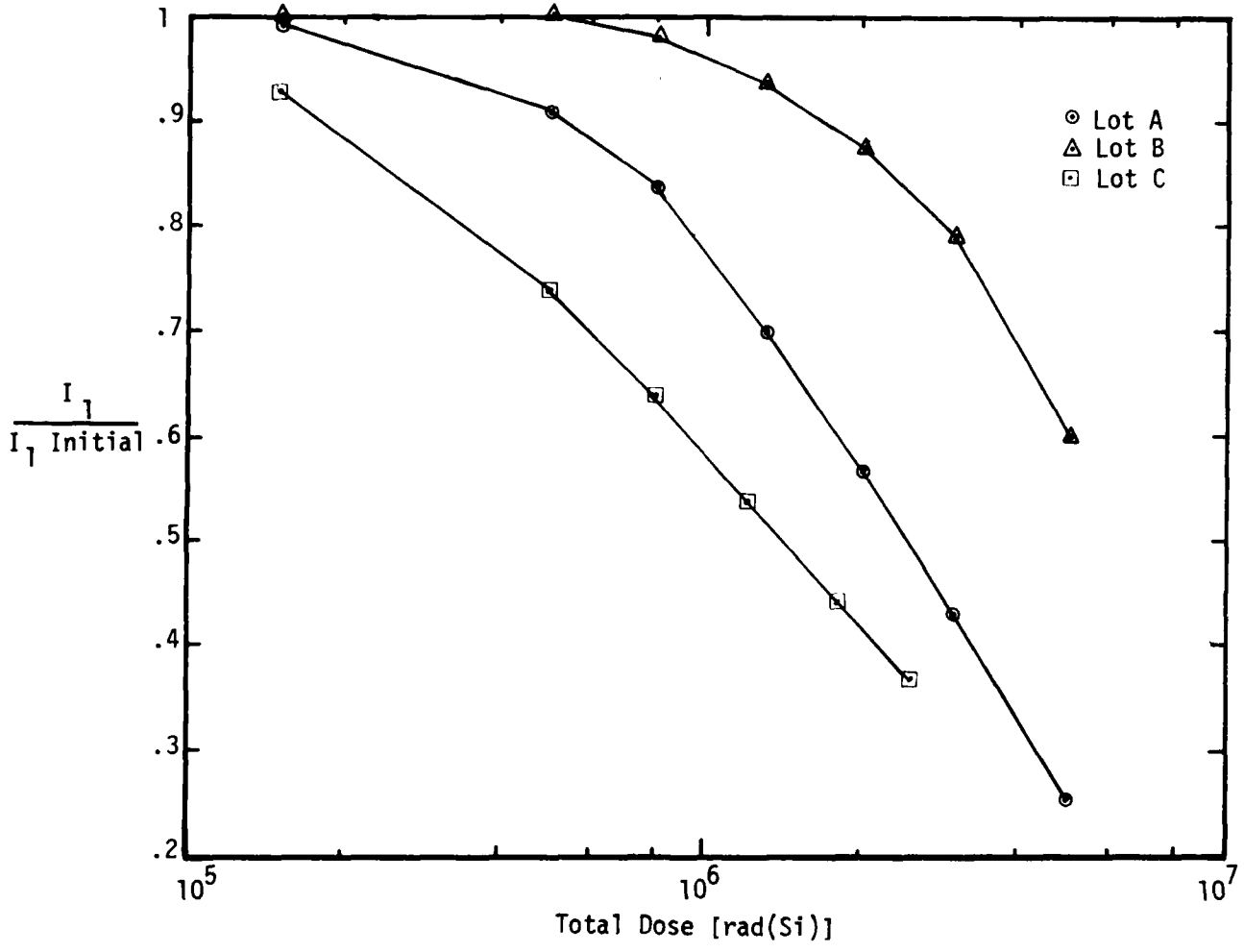


Figure 11. Change in first stage current with total dose.

6-2 EFFECT OF ELECTRICAL SPECIFICATIONS ON DEVICE HARDNESS.

One of the motivations for this study was the need to investigate the feasibility of using "reject" devices that do not meet the electrical specifications over the entire temperature range as radiation test samples. This is important because the yield of 108A devices is low—so low in fact that, for some wafers, a small radiation test sample would seriously deplete the number of 108A devices. Wafer-level testing is not practical in this case unless other devices, such as 308A or 108 circuits, or breakout transistors can be used as test samples.

Careful examination of the radiation data showed that only slight differences occurred between the device categorization as a 108A, 308A, or 108 circuit and the radiation response. This comparison is limited by the small, variable number of 108A devices, and it was necessary to combine wafers from the same diffusion lot in order to increase the number of 108A devices so that a meaningful comparison could be made. Figure 12 compares ΔV_{OS} for different device categories from two diffusion lots after exposure to approximately 1.2 Mrad(Si).

The 108A devices from lot C are slightly harder than the 308A devices from that lot. Although there are approximately equal numbers of 308A and 108 devices from lot C, there were more 108A devices from the harder of the two wafers. The apparent difference in the 108A radiation response is due to the unequal number of 108A devices from the two wafers. Within the limits imposed by the small number of 108A devices, there appears to be no significant difference in the radiation response and the initial device categorization for any of the eight wafers. The input bias current was also examined for each wafer, and is consistent with this conclusion. Therefore, commercial fallout parts can be used as radiation test samples for lot sample testing.

Note however that the major cause of reject devices was failure to operate within specification at extreme temperatures. There were no consistent differences in the room temperature specifications of the different circuit categories, and the electrical parameters of these circuits were closely matched. If consistent differences in initial input bias current or internal current source values occurred between these device categories, this could cause significant differences in the radiation response. Before using commercial devices as radiation test samples, their electrical specifications should be compared with those of the high tolerance devices to make sure that no significant differences occur.

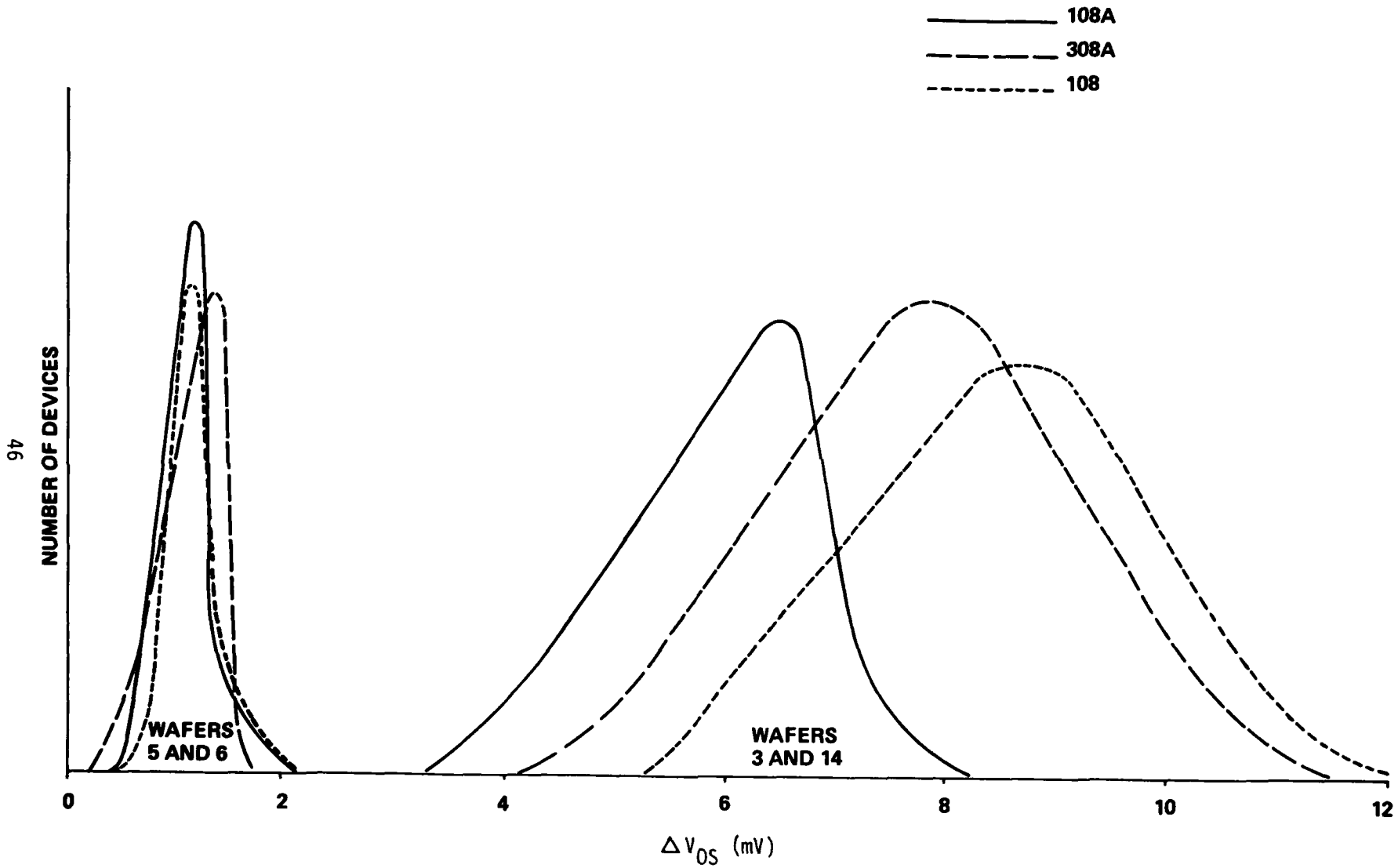


Figure 12. Comparison of offset voltage changes for 108A, 108 and 308A devices.

6-3 HOMOGENEITY RESULTS FOR CIRCUITS.

It is clear from the preceding results for the breakout transistors that only slight differences occurred between the radiation hardness of wafers from the same diffusion lot. Therefore, the circuit homogeneity will be examined on a diffusion lot basis. There are difficulties in making quantitative comparisons among the circuits because of the importance of all four internal transistor types to the circuit response mechanisms. However, the final test of circuit homogeneity is the distribution of the key circuit parameters—particularly V_{OS} and I_B—after irradiation, and this approach will be used to examine circuit homogeneity.

In order to increase the number of devices beyond the limited number of 108A circuits, the 308A, 108 and 308 devices were included in the homogeneity comparison. The results of the previous section have shown that the radiation response of these devices do not depend on their initial electrical parameters.

The change in input bias current after irradiation to a level of approximately 2 Mrad(Si) is shown in Figure 13. The data for diffusion lots A and B are grouped together in the histogram because they had similar responses. The differences among the three lots closely follow the relative hardness of the super-β transistors, as expected. The first-stage current source response is also important. The range of ΔI_B at this level is approximately a factor of 2 within a given diffusion lot. However, one device from diffusion lot C (wafer 14) was substantially harder than the other devices in this group. This device was consistently harder at all radiation levels, and there were no obvious differences in its initial electrical parameters that would indicate abnormal internal bias currents.

A similar figure for ΔV_{OS} is shown in Figure 14. The increased sensitivity of diffusion lot C is clearly evident from this figure and the range of ΔV_{OS} for most of the devices from this diffusion lot is a factor of 2. However, there are two devices from lot C with much smaller V_{OS} changes. There is also one device from lot A which has an unusually high change in V_{OS} at this level. Two devices from lot B had a negative V_{OS} change, which became smaller at higher radiation levels.

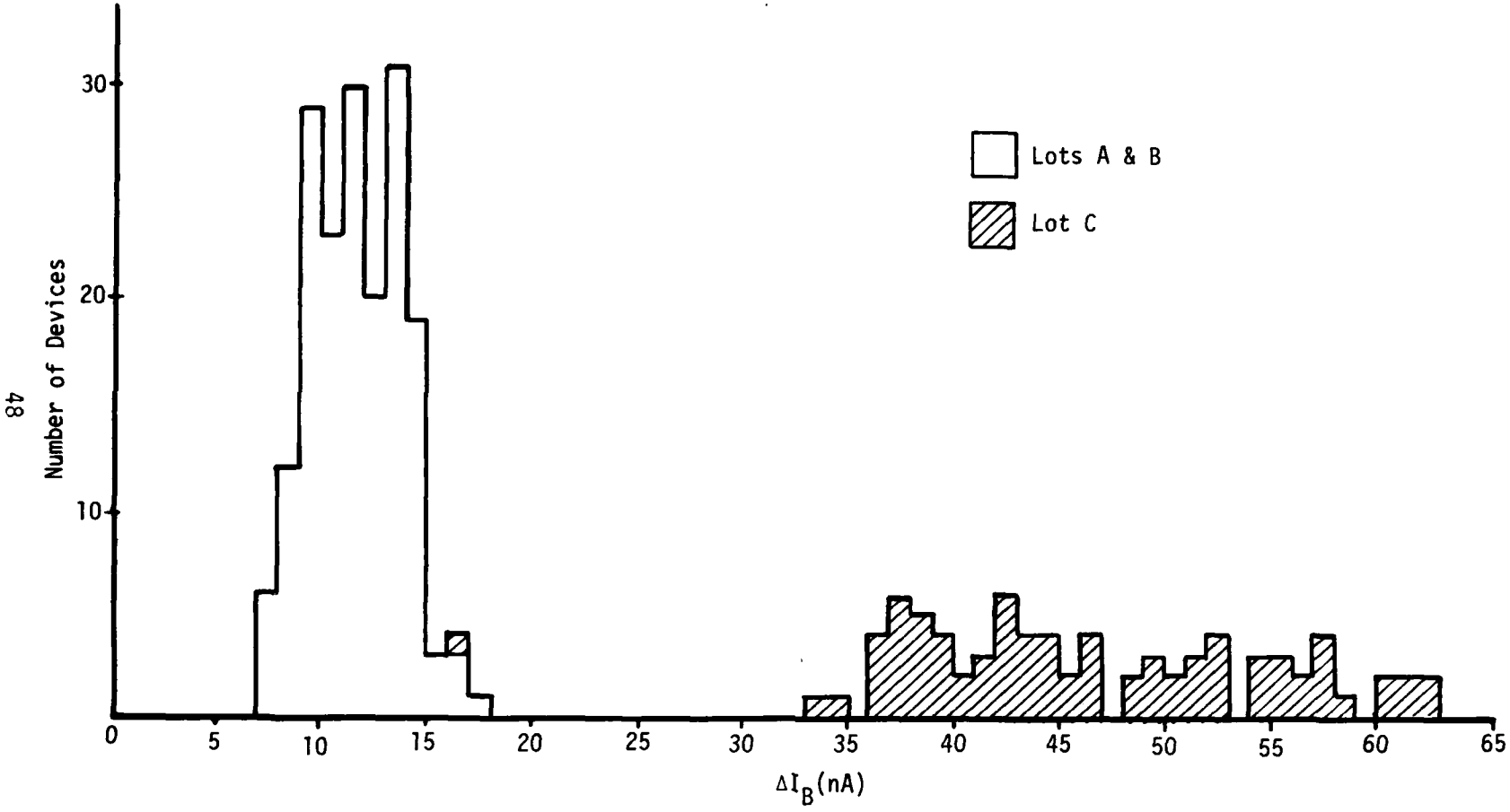


Figure 13. Histogram of input bias current changes for the three diffusion lots.

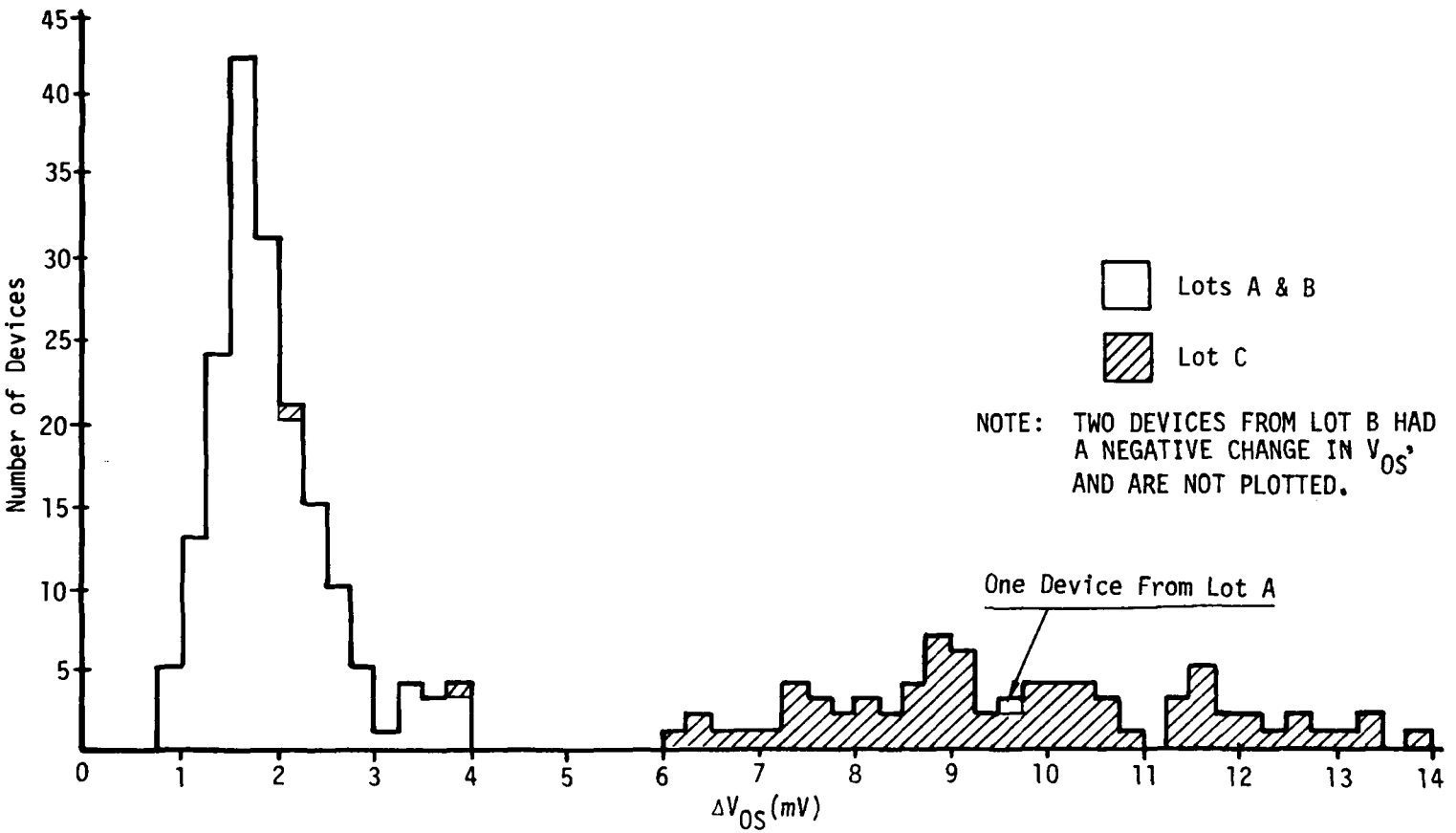


Figure 14. Histogram of offset voltage changes for the three diffusion lots.

Clearly the existence of small numbers of devices with extreme changes in electrical parameters is of great concern to hardened systems. The test data of these three atypical devices were examined in detail to make sure that the data are valid, and to determine the mechanisms responsible for their different response to the radiation environment.

Examining the two hard devices from lot C, one of these devices was the same unit which exhibited a lower ΔI_B in Figure 13. This device is clearly harder than the other devices from this lot; both I_B and V_{OS} change smoothly with radiation, and are substantially below the changes of the other devices at all levels. The other device from lot C had a second mechanism that affected V_{OS} at low levels. This mechanism caused V_{OS} to initially change in a negative direction. At 800 krad(Si), ΔV_{OS} for this unit was -19 mV. Above this level, V_{OS} changed in a more positive direction, and the reason for the low offset voltage change in Figure 14 is the near cancellation of these two mechanisms. The same mechanism was observed for the two devices in lot B.

The responses of the three devices which exhibited this negative V_{OS} change are compared with the mean response of other devices from their respective wafers in Figures 15 and 16. Note that the initial negative response occurs at low radiation levels, and appears to saturate. At higher levels, the positive ΔV_{OS} mechanism identified in Section 5 dominates, causing the offset voltage change to go through zero. The mechanism that causes this negative response has not been identified, but may be due to internal transistors with excessive leakage currents.

The more sensitive device from lot A also changed in a smooth way with increasing radiation levels. There is no evidence of oscillations or experimental errors that would affect this data. The increased sensitivity of V_{OS} for this device appears to be valid, and is apparently caused by the same mechanism as the other devices in that diffusion lot. Since ΔI_B changed in the same way as other devices from lot A, there is no possibility that the increased offset voltage sensitivity is due to accidental mixup of the wafer identity of this device.

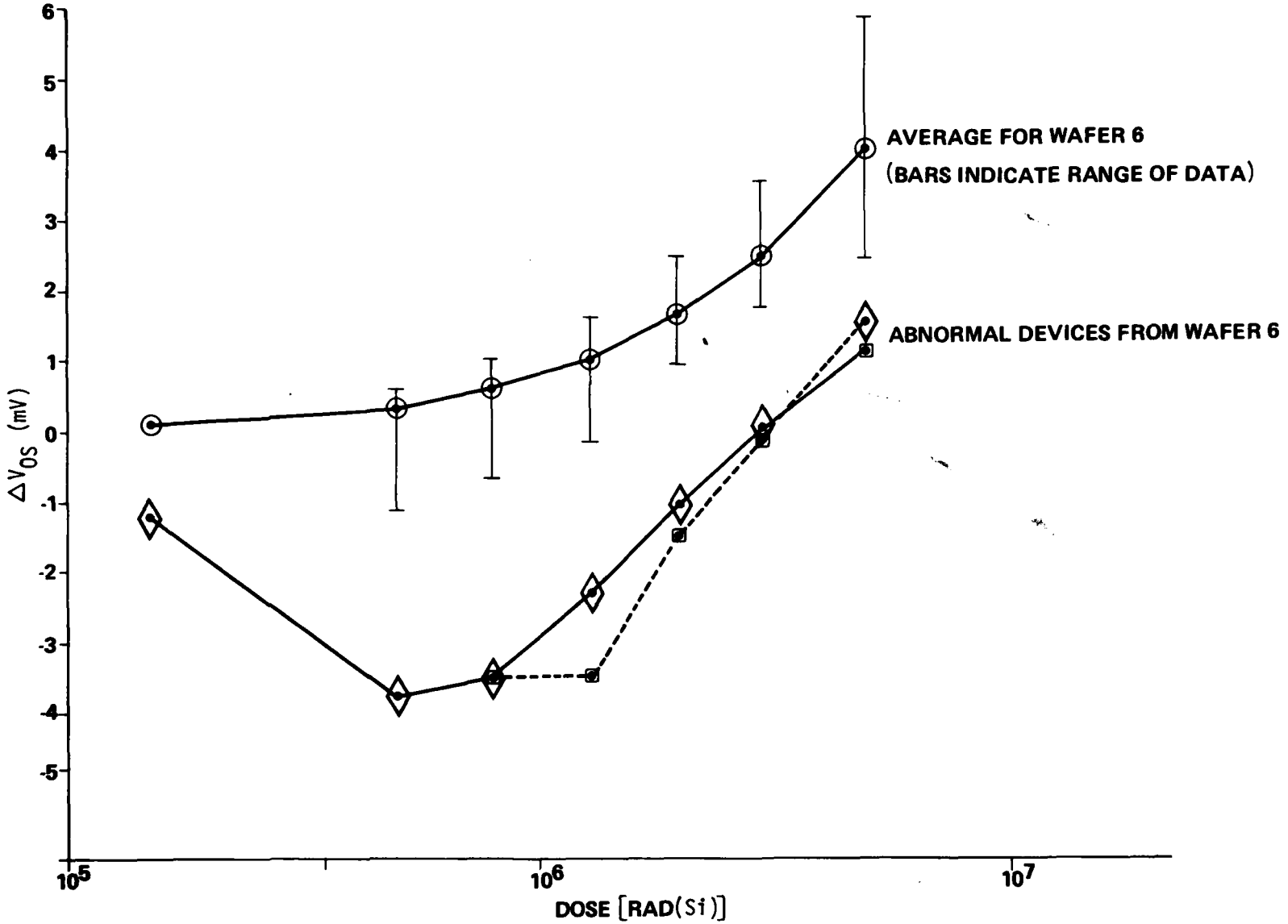


Figure 15. Comparison of abnormal and typical device responses for wafer 6.

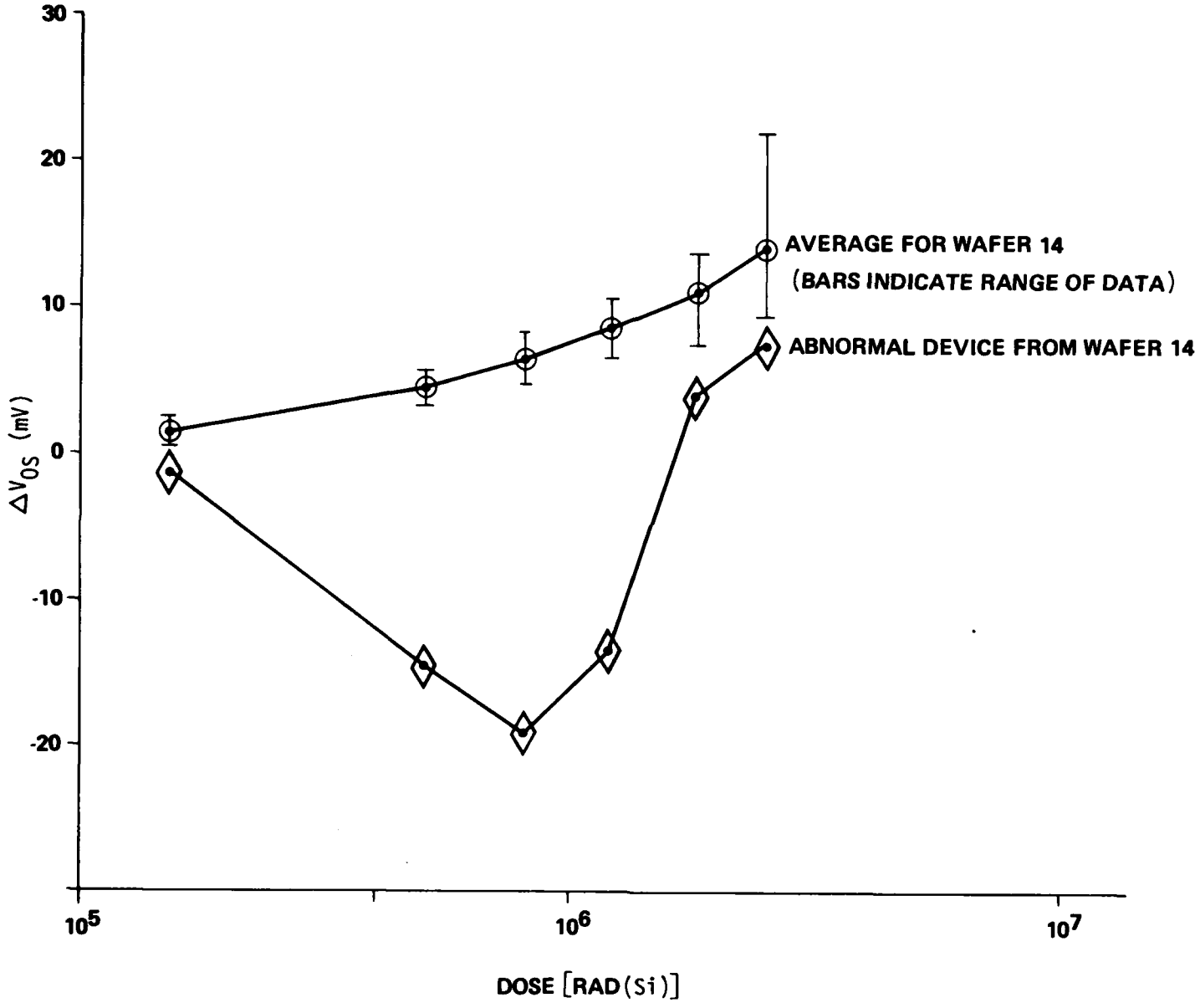


Figure 16. Comparison of abnormal and typical device responses for wafer 14.

During the irradiation, offset voltages were initially measured in the radiation test fixture, using an external voltmeter. These measurements were made to provide V_{OS} data immediately after irradiation as a check on annealing. Complete characterization was done a few minutes later using the automated test system. Comparison of the V_{OS} data taken in those two independent methods provides a secondary check on the validity of the data. These measurements were carefully cross-checked for the three devices with abnormal behavior, and were consistent. Therefore, one must conclude that these V_{OS} changes are real, and are not due to experimental difficulties.

These data show that the majority of circuits from a single wafer or diffusion lot are well behaved in a total dose environment with a relatively narrow distribution. However, a small number of devices deviate substantially from the population majority. Approximately one percent of the devices fit this category, which is a large enough fraction to seriously affect system hardness. Fortunately none of the devices failed catastrophically, so that they would work in many system applications even with the larger radiation response. More work needs to be done to identify the failure mechanisms and to develop screening methods to eliminate these devices.

SECTION 7

X-Y TRACEABILITY RESULTS

7-1 WAFER GEOMETRY.

As discussed in Section 3, two wafers were obtained with x-y coordinate traceability in order to study subwafer homogeneity. One wafer, number 76, was selected from diffusion lot A, and the other, number 2, from diffusion lot B. These wafers were selected after wafer probing, prior to assembly. Although their yields were known after probing, there was no way to predict the yield after assembly. Circuits which passed electrical specifications after assembly tended to be located in random locations on the wafer, so that only limited information about short range homogeneity could be obtained from the circuits.

These wafers contained three horizontal rows of breakout transistors. For the x-y study, the entire center row of breakout transistors was assembled, alternating the two bonding patterns. Although a few of the transistors had electrical abnormalities and were not tested, the breakout transistors provide a nearly continuous sample across one axis of the wafer. The transistors provide a means of testing the short term radiation variability that cannot be achieved with the low-yield circuits, which are located in more random positions.

The wafer locations of circuits and breakout transistors used for the x-y study are shown in Figures 17 and 18. The devices which appear in subsequent figures in this section are delineated on these figures, along with the type of circuit (108A, 308A or 108). All types of circuits were included in the x-y study in order to obtain maximum information about subwafer homogeneity. The irradiation and testing procedures used for the wafers with x-y traceability were the same as those used for the other wafers in the study.

7-2 BREAKOUT TRANSISTOR RESULTS.

There was a marked difference in the local homogeneity of the transistors from the two wafers with x-y traceability. This occurred for both the pre-irradiation electrical characteristics and the radiation damage. Systematic variations were observed for transistors from wafer 2, whereas those of wafer 76 were relatively uniform across the wafer. The variation with wafer position was most pronounced for the super-β and substrate PNP transistors. For example, the pre-irradiation gain of the super-β transistors from wafer 2 ranged from 1800 to 5500 across the wafer, compared to $\pm$10 percent variability observed for wafer 76.

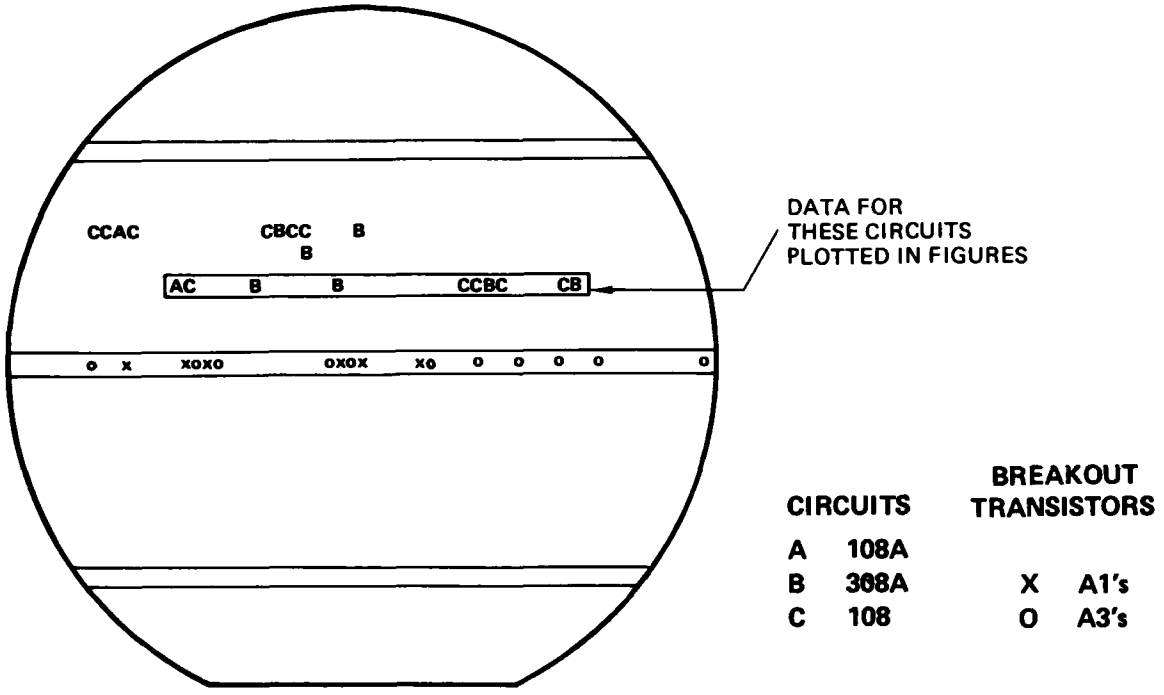


Figure 17. Wafer locations of circuits and transistors from wafer 76.

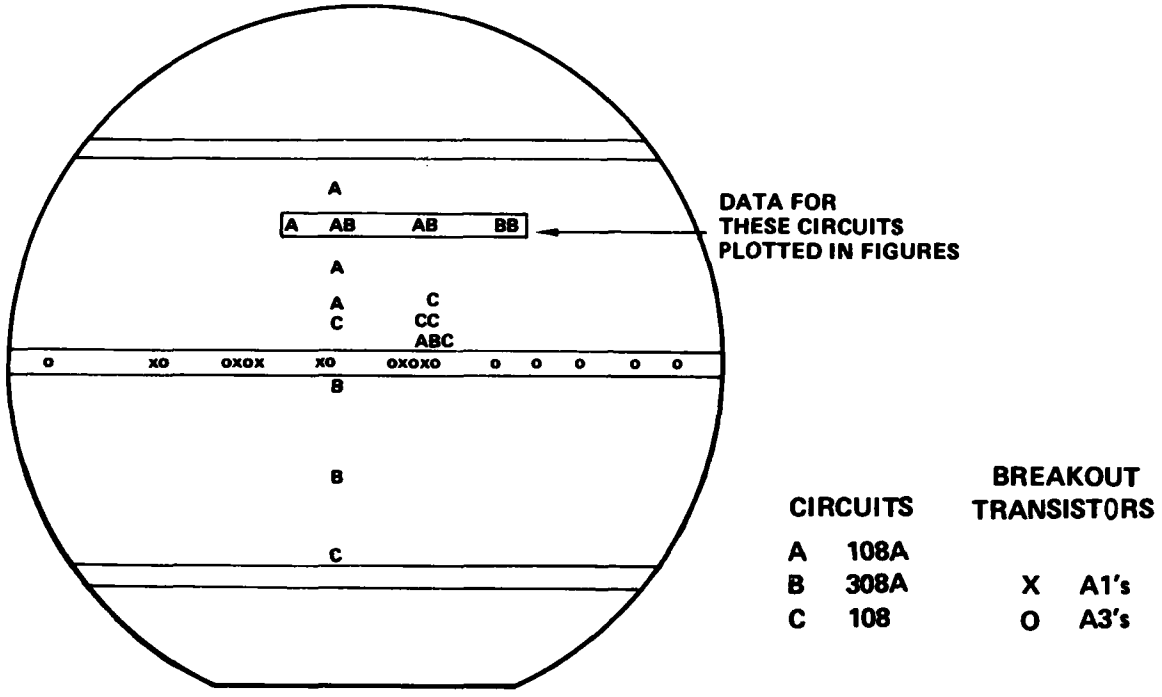


Figure 18. Wafer locations of circuits and transistors from wafer 2.

Figures 19 and 20 show the variation of Δh_{FE}^{-1} with wafer position for the four types of breakout transistors after exposure to a fluence of approximately 1 Mrad(Si). The radiation-induced damage of the super-β and substrate transistors from wafer 2 varied systematically with position, whereas those of wafer 76 were relatively uniform across the wafer. The maximum differences were approximately a factor of 3 for the super-β transistor and a factor of 2 for the substrate transistor. Devices at the extreme edges—16 or 17 die from the wafer center—were not included, because they often had abnormal pre-irradiation gain. None of the circuits at the extreme edges were electrically functional for any of the eight wafers in the study, including the two x-y wafers. The other two transistor types exhibited more uniform behavior across both wafers. The lateral PNP transistors were particularly uniform.

There was an inverse correlation between the initial gain of the transistors and the damage factor. This was particularly evident for the substrate transistors, which for wafer 2 showed gain variations of 35 percent across the wafer, with the same systematic variations evident in the total dose damage data. The initial gain of this transistor is strongly dependent on the epitaxial layer thickness, which affects the base width, and this may not be uniform for all wafers.

The data on the two x-y wafers demonstrate that wafer homogeneity is not consistent between different wafers. Although the maximum observed differences in Δh_{FE}^{-1} are not large, the factor of 2 to 3 in gain degradation will result in much larger differences in the terminal behavior of 108A circuits, as discussed in Sections 5 and 6. (A factor of 3 variation in Δh_{FE}^{-1} of the super-β transistor causes nearly a factor of 10 difference in the radiation failure threshold.) In order to reduce this variability, wafer traceability would have to be maintained over small fractions of the wafer area. The short-range homogeneity is not much better than the wafer homogeneity unless the die range is restricted to approximately 10 die. For low-yield devices such as the 108A, very small numbers of circuits would be obtained from such local areas, limiting the applicability of subwafer traceability.

7-3 CIRCUIT RESULTS.

The x-y data for the 108-type circuits exhibited the same subwafer dependence as the breakout transistors. The radiation response of wafer 76 was relatively uniform with variations in horizontal position, whereas that of wafer 2 varied with position. Figures 21, 22 and 23 show the variation of ΔV_{OS}, ΔI_B, and

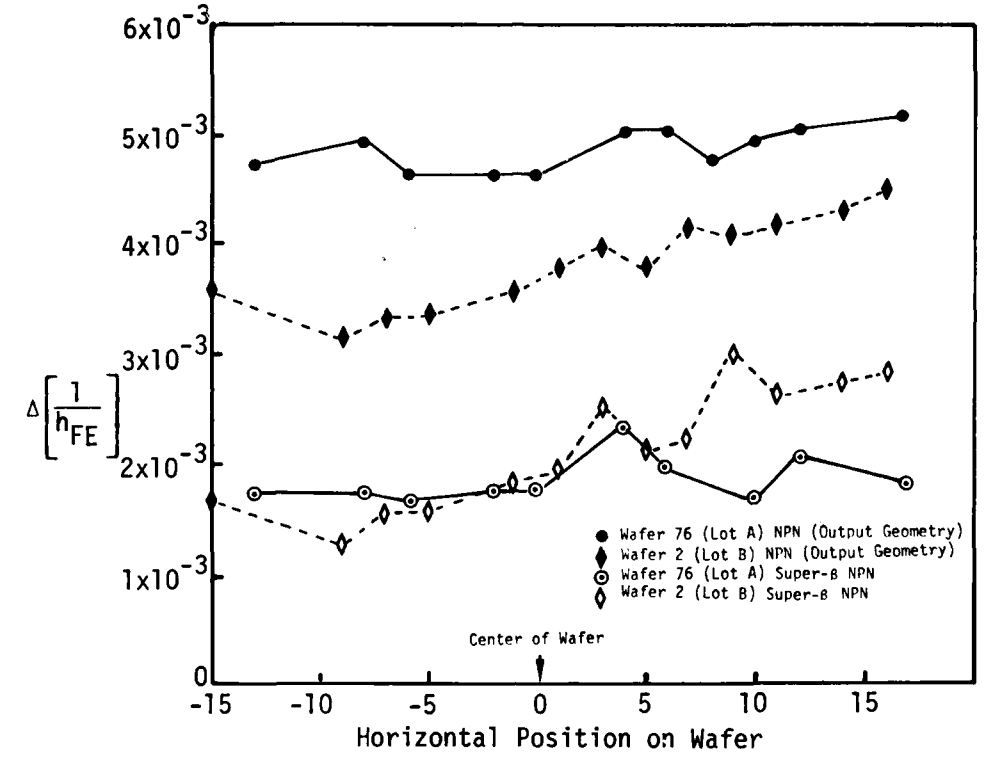


Figure 19. Subwafer dependence of Δh_{FE}^{-1} for NPN transistors.

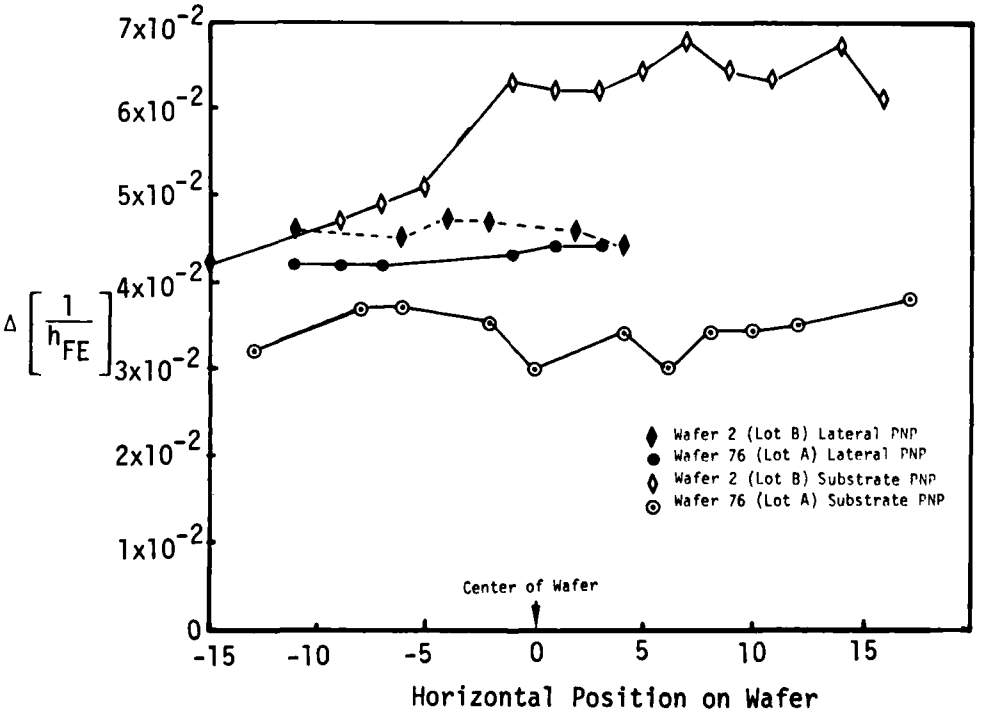


Figure 20. Subwafer dependence of Δh_{FE}^{-1} for PNP transistors.

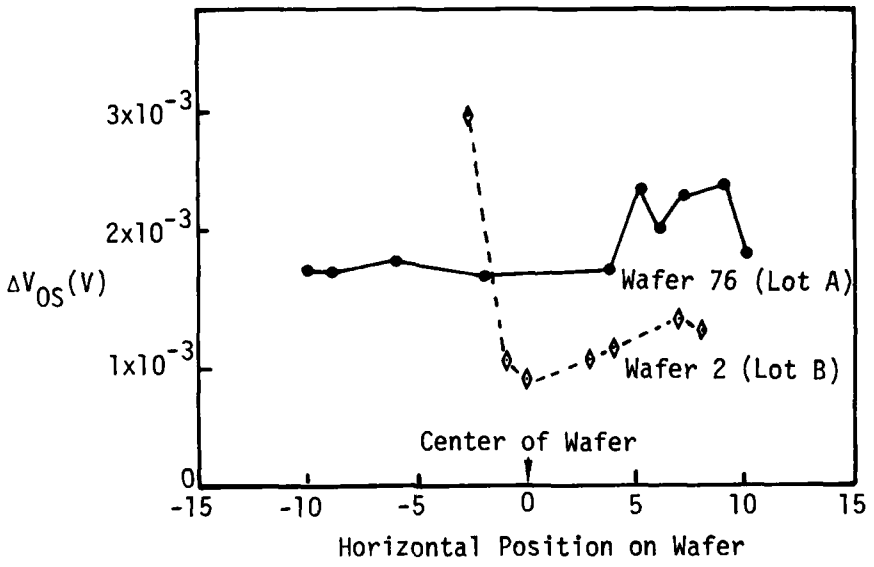


Figure 21. Subwafer dependence of ΔV_{OS} for circuits.

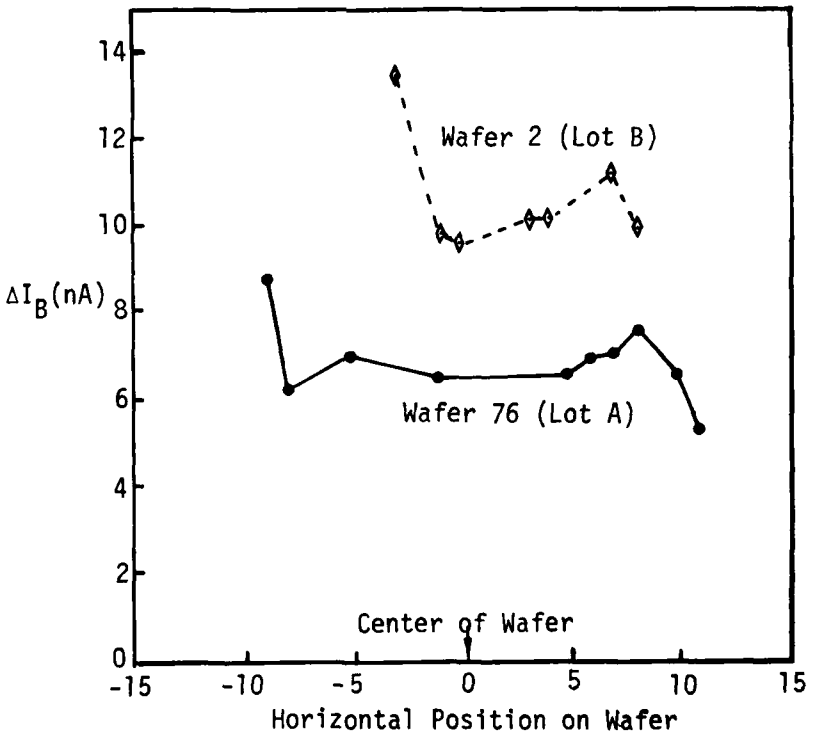


Figure 22. Subwafer dependence of ΔI_B for circuits.

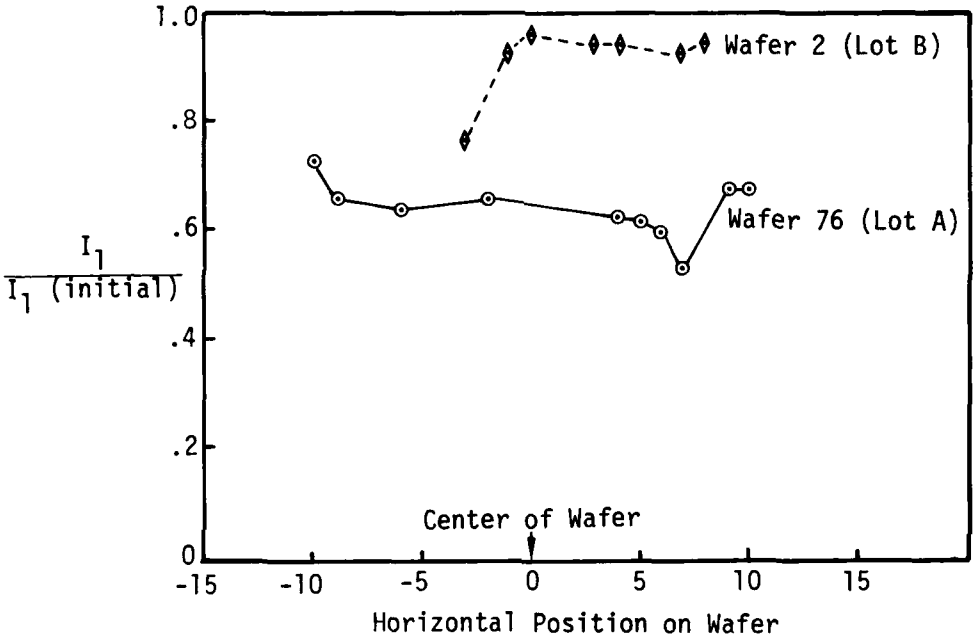


Figure 23. Subwafer dependence of I_1/I_1 (initial) for circuits.

the fractional remaining first stage current ($I_1/I_{1(o)}$) as a function of horizontal position. The exact wafer locations of these circuits are shown in Figures 17 and 18. The probe yield of circuits from wafer 2 fell to zero just to the left of the center of the wafer, which limited the horizontal range over which its uniformity could be evaluated, although breakout transistors were obtained over the entire horizontal position of the wafer. The data in Figures 21 through 23 show a larger radiation response for the device at the edge of this yield boundary, although the difference is not large enough to be significant for most applications. Since the yield fell to zero to the left of this device, one can conclude that the normal electrical specifications are effective in limiting such systematic variations in radiation hardness.

Although not shown, radiation data on circuits with different vertical wafer locations were similar to the horizontal cross section plotted in Figures 21 through 23. The location of these circuits are shown in Figures 17 and 18. The devices from wafer 2 exhibited smaller differences in the vertical than in the horizontal direction, whereas circuits from wafer 76 behaved similarly in the horizontal and vertical directions.

The x-y traceability results show that subwafer homogeneity is substantially better than homogeneity over the entire wafer. However, for these devices the degree of improvement obtained with subwafer traceability is probably too small to justify the cost and production control problems required. The short-range homogeneity results show that local test structures on each individual chip (or the use of adjacent devices as test structures) could be effective in further reducing the hardness variation of <u>typical</u> devices. As discussed in Section 10-3, this approach would probably not be effective in controlling the abnormal devices observed in this program. Before this approach could be used, a suitable electrical screening method would have to be developed. The testing could be done at probe, or on extra circuit leads provided for this purpose.

It should be noted that the concept of subwafer traceability may be more compatible with circuit types that have higher yield over small areas than the 108A. This circuit is extremely difficult to fabricate successfully, primarily because of the combination of tight electrical requirements and wide temperature requirements. The short-range variability of the breakout transistor radiation response would probably be comparable for other linear devices made by AMD, and can be used as the basis for evaluating the applicability of subwafer traceability to other circuit types.

SECTION 8

ANNEALING EXPERIMENTS

8-1 LONG TERM ANNEALING.

Space systems are usually exposed to ionizing radiation over time periods which are much longer than those used for simulation studies. Because total dose damage anneals with time, data from simulation studies may be overly conservative for space system applications. Unfortunately the annealing results for bipolar devices are not consistent for different device types and it is difficult to estimate annealing effects unless data are available for the actual devices under consideration. Only limited data are available on annealing effects in modern linear devices that use several unusual transistor structures (see Section 2).

An annealing experiment was completed which examined circuit annealing behavior in the time period from 0.15 to 1000 hours after an initial irradiation to 5×10^6 rad(Si). Bias was applied on these devices during the entire 1000 hours of the experiment and all annealing occurred at room temperature ($22 \pm 3°C$). The devices were periodically retested to examine the annealing.

The annealing behavior was fitted to the equation

$$\Delta(\text{parameter})_t = A\, t^{-n}, \tag{8}$$

where n is an empirical constant and A is a constant which corresponds to the largest change in the parameter at t = o. For short times, this can be written as

$$\Delta(\text{parameter})_t = Ae^{-n \ln t} = A\left(1 - n \ln t + \frac{n^2(\ln t)^2}{2} - \ldots\right)$$

so that

$$\Delta(\text{parameter})_t \simeq A(1-n \ln t) = A\left(1 - \frac{n \log t}{2.303}\right) \tag{9}$$

The parameters that changed most significantly with time were I_B, I_{OS}, and V_{OS}. Only slight change were observed for the parameters A_{OL}, I_1, and I_{SINK}, and none of the other measured parameters changed significantly during the annealing experiment.

Annealing data for I_B are shown in Figure 24. These data fit equation 9 reasonably well, and even at 1000 hours the curve does not depart from the straight line predicted by equation 9 for small t. For ΔI_B, the slope of the logarithmic dependence on time was n = 0.06. Data for I_{OS} exhibited the same slope, although there was more scatter in the data points; this is expected because I_{OS} depends on the difference in the bias currents of the two input parameters, and cannot be measured with the same accuracy.

The input offset voltage annealing behavior was not as straightforward. Figure 25 shows the annealing of ΔV_{OS} with time. There is an initial increase in ΔV_{OS} during the first hour, which is inconsistent with the decrease that occurs at longer times. The reason for this behavior is not completely understood, but there may be competing mechanisms with different time dependence. One complicating factor is the temperature dependence of V_{OS}, which shows large increases after total dose irradiation. Typical preirradiation temperature coefficients for V_{OS} are in the range 1-5 μV/°C; after exposure to 5 Mrad(Si) this coefficient increased to approximately 35 μV/°C, and is large enough to significantly affect the offset voltage measurements. The internal temperature of the ^{60}Co irradiation cell is approximately 8°C above ambient temperature, which may account for the low ΔV_{OS} values immediately after irradiation.

Another concept which is useful in describing annealing effects is the annealing ratio (AR). This ratio is defined by

$$AR = \frac{\Delta(\text{parameter})_t}{\Delta(\text{parameter})_{t_{ref}}} \tag{10}$$

where t is the time at which the value of the annealing ratio is calculated and t_{ref} is a normalization time (1000 hours for this data). This is similar in concept to the annealing factor used to describe neutron damage in transistors. However, the annealing ratio is not expected to be the same for different parameters or different circuit types because the measured parameters do not change linearly with total dose, and the gain of the internal transistors is not linearly dependent on total dose damage. Although it is a useful way to look at annealing, the AR in a total dose environment is an empirical concept that lacks the fundamental linearity of the neutron annealing factor.

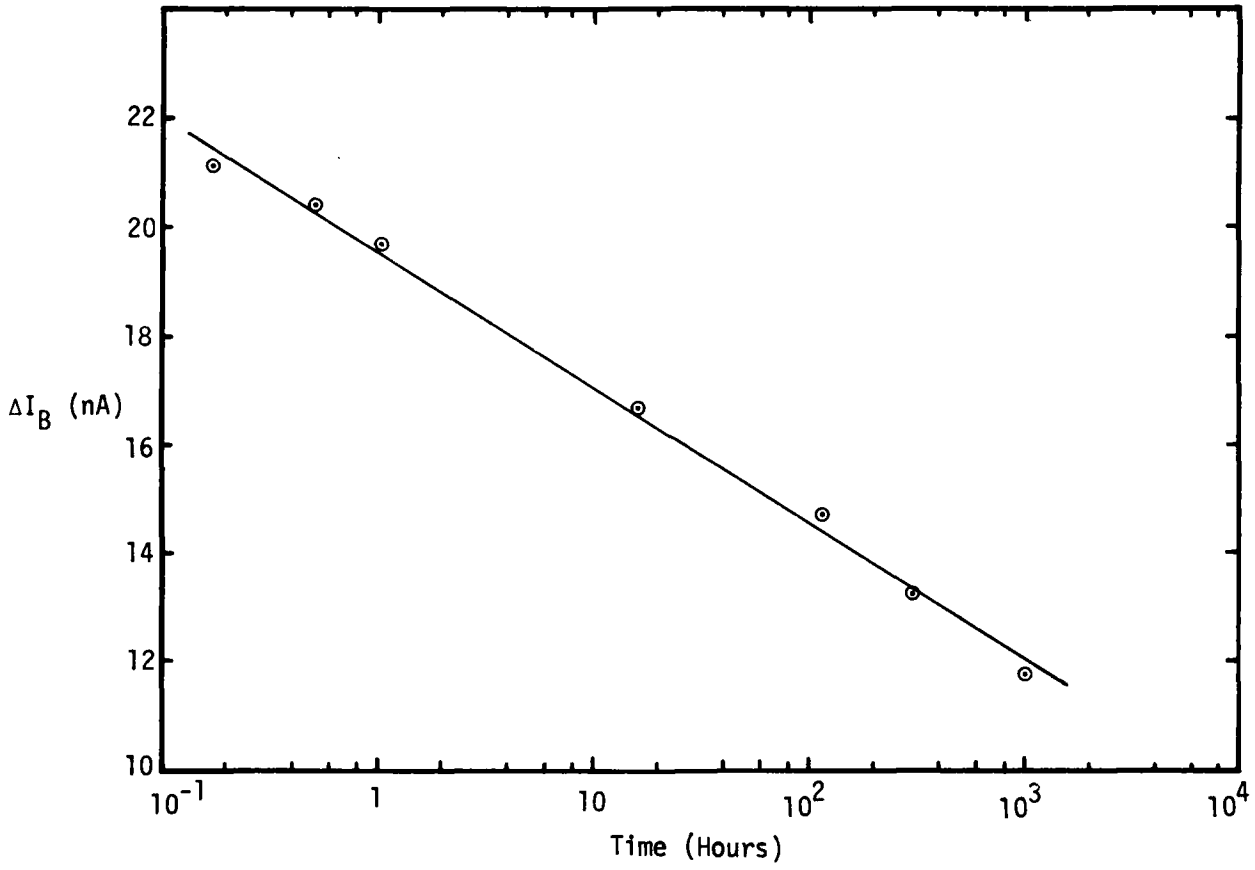


Figure 24. Long-term annealing of input bias current.

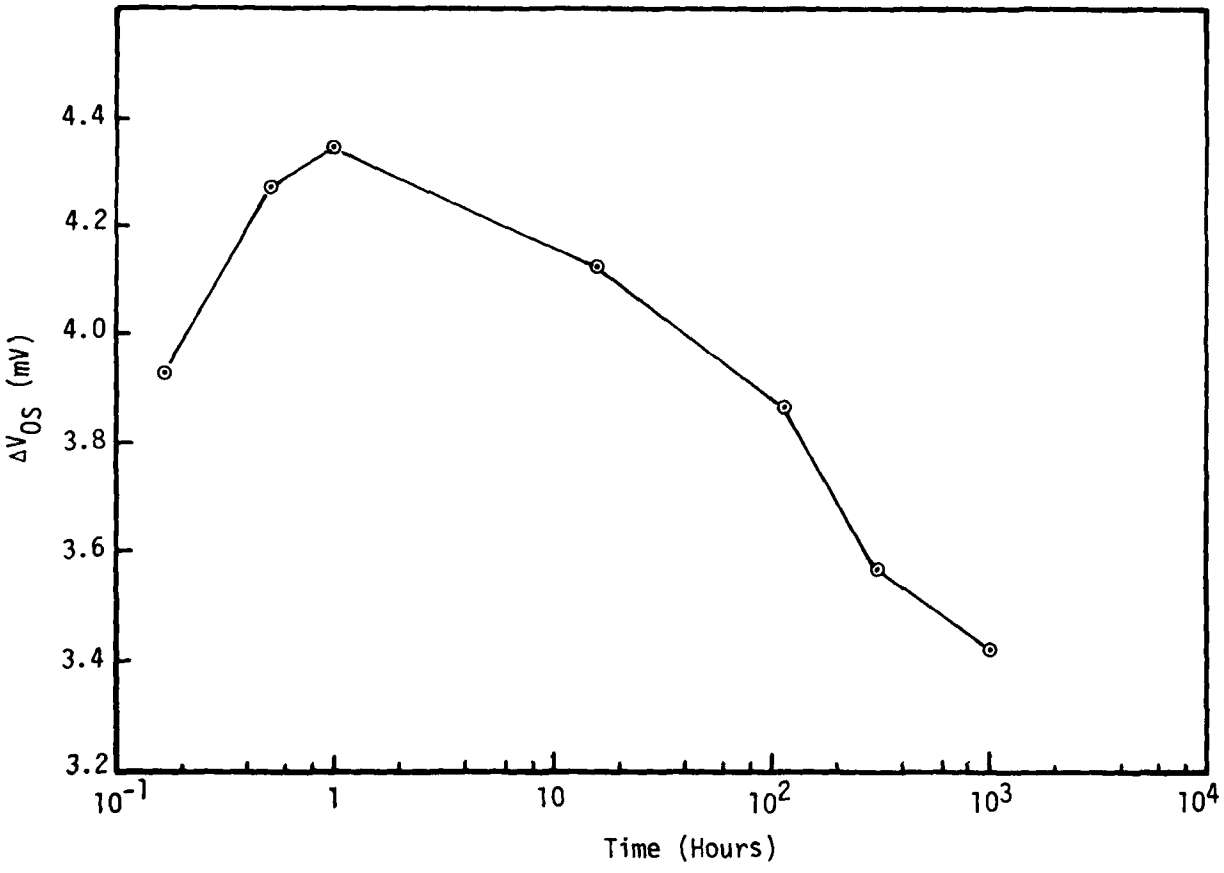


Figure 25. Long-term annealing of offset voltage.

The annealing ratios for the parameters V_{OS}, I_B and I_{OS} are plotted in Figure 26. The relative change in I_B and I_{OS} is approximately a factor of 2 during the first 1000 hours and is much larger than the change in V_{OS}. These data are useful in applying component data taken at short times to satellite systems which may have extremely long irradiation times. However, it should be noted that annealing effects may be temperature dependent and these data apply only to room temperature.

8-2 CONSTANT-IRRADIATION TIME EXPERIMENT.

The ^{60}Co irradiation cell has a fixed activity and therefore the total dose level of exposed devices is varied by changing the time of exposure. The minimum irradiation time used for any of the devices on this program was 11 minutes and the maximum time for an incremental fluence level was 2-1/2 hours. In order to make sure that annealing or charge redistribution did not affect the fluence dependence of damage, an additional experiment was completed which used a constant irradiation time of 1000 seconds. Data from this experiment can be compared with the ^{60}Co irradiation data to determine the effect of the variable irradiation time. The Boeing Dynamitron was used as a radiation source for this experiment. The current density of the 2.2 MeV electron beam was adjusted for each radiation level to give the required dose in the 1000 second time interval.

The results of this experiment were essentially identical to the ^{60}Co irradiation results for devices from the same wafers, as shown in the data of Figure 27. Good agreement was obtained for both the damage and the slope of Δh_{FE}^{-1} at the different radiation levels, which demonstrates that annealing effects did not change the results during the time intervals associated with the irradiation. Therefore, the varying exposure time of the ^{60}Co irradiations does not affect the fluence dependence.

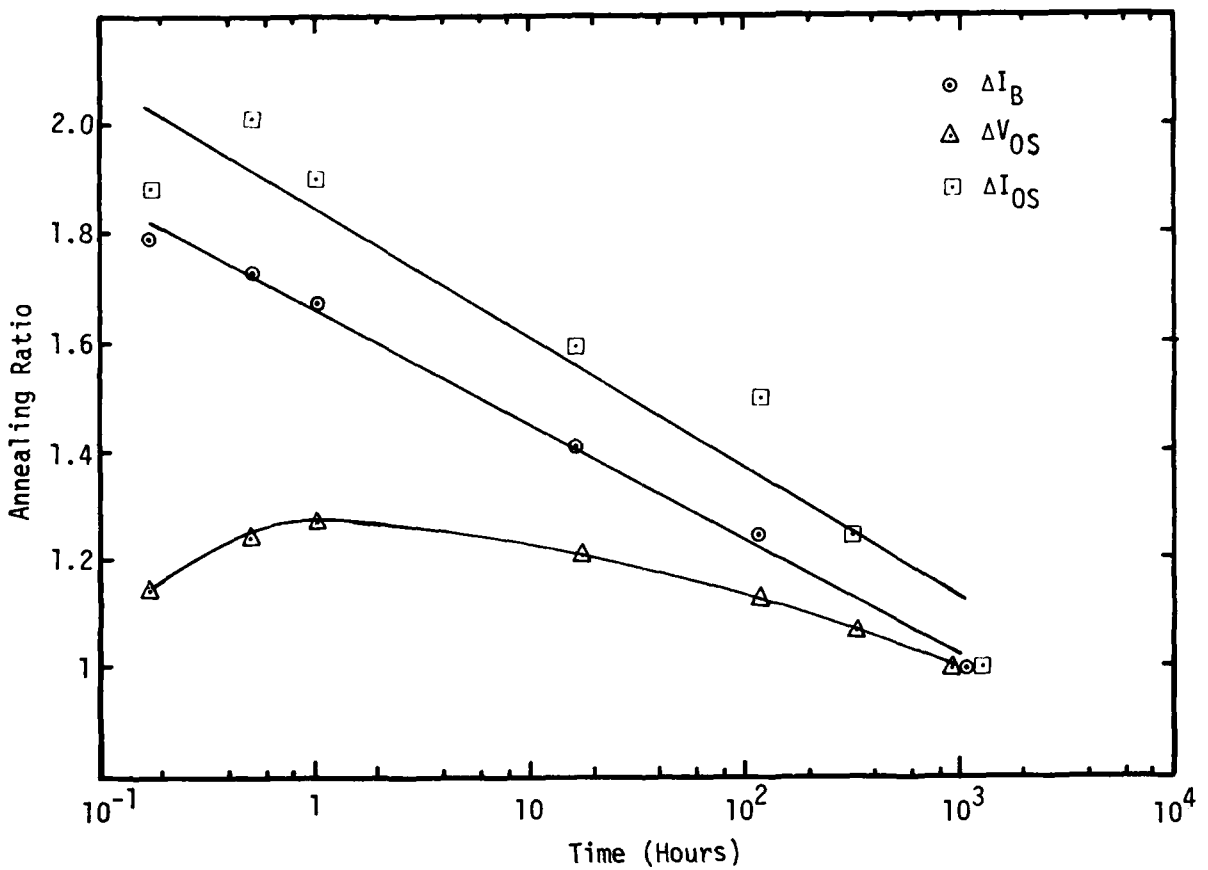


Figure 26. Annealing ratios of offset voltage, bias current and offset current.

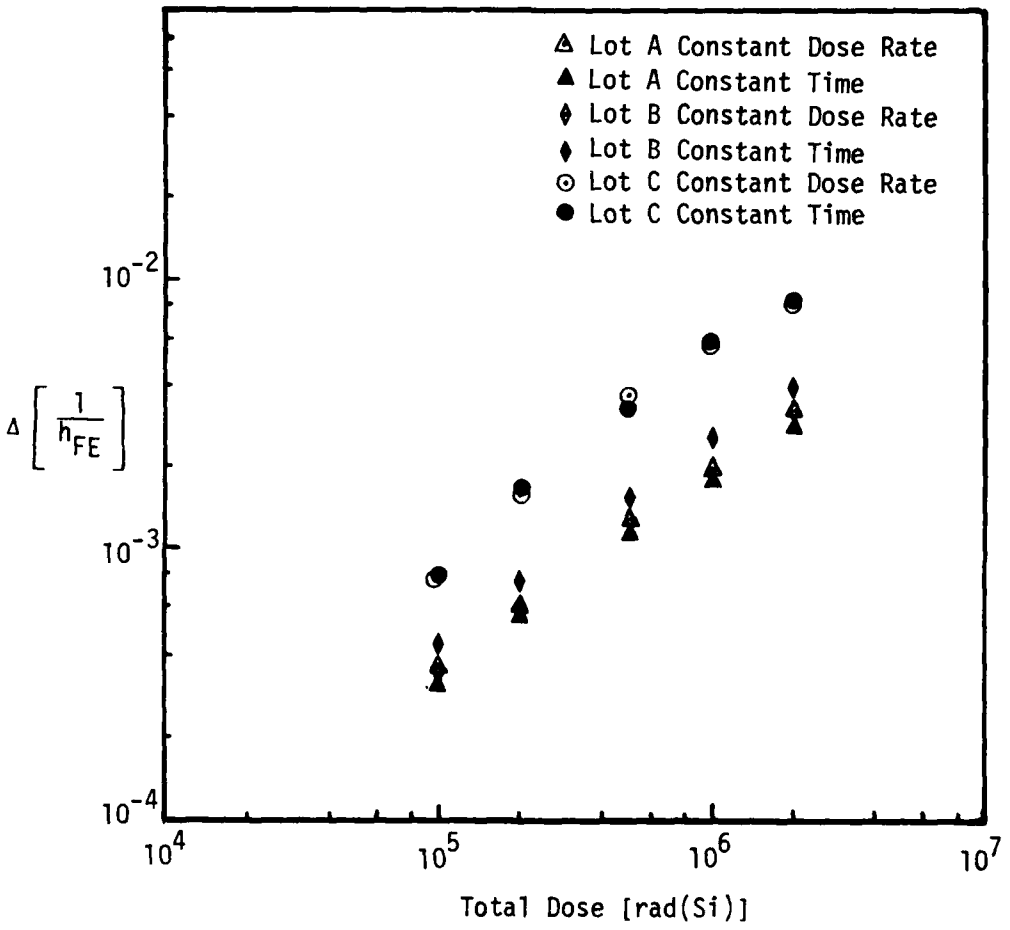


Figure 27. Δh_{FE}^{-1} comparison with different radiation rates.

SECTION 9

EXPERIMENTAL DETAILS

9-1 RADIATION SOURCES.

The radiation source used for all experiments (except the constant-irradiation period experiment) was a Gammacell 220 ^{60}Co irradiation cell. This cell consists of an annular source, shielded by a lead enclosure, which provides uniform dose within a cylindrical irradiation cavity. The dimensions of the cavity are 15 cm in diameter by 20 cm high. At the time of this contract, the activity of the cell was approximately 1.3×10^4 rad(Si)/min. An elevator assembly with an integral timer automatically lowers the experimental assembly into the cavity for a prescribed time interval. A shielded tube provides access for wiring so that power may be applied to devices during irradiation.

For the constant-irradiation period experiment, 2.2 MeV electrons from the Boeing Dynamitron accelerator were used. This is a direct current particle accelerator which produces a constant flux of electrons; the maximum current is 10 mA in the electron mode. The test devices were located approximately 6 cm from the primary beam during irradiation.

9-2 TEST FIXTURES.

A battery-powered mobile bias fixture was used to provide active bias for the circuits during and after irradiation. The circuits were connected as active amplifiers (A_V = 100) with supply voltages of $\pm$15 V. Monitor points were provided so that input offset voltage could be quickly measured after irradiation. This provided a check on possible fast annealing of radiation damage.

Small circuit boards were used to hold the devices during irradiation. These circuit boards were provided with contacts at each end so that the devices could be plugged into the electrical test fixture with only momentary interruptions of bias. The radiation test fixture was designed to hold a maximum of 20 devices. A schematic diagram of the test fixture card is shown in Figure 28.

A similar test fixture was used for the breakout transistors, but it held only six devices. The wiring and biasing of the transistors was more complicated because there are three transistors within each package. Initial tests were done using both reverse and forward bias. A schematic of the test fixture

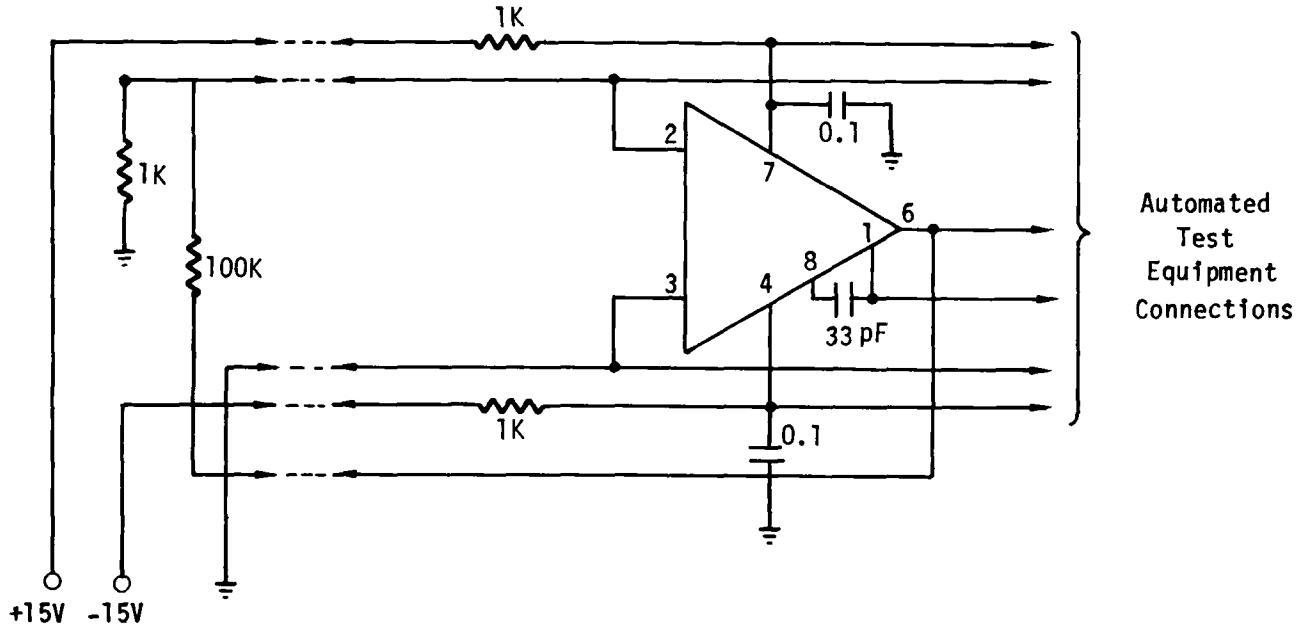


Figure 28. Electrical schematic of circuit test fixture.

is shown in Figure 29. The voltages shown are for moderate forward bias which approximated the conditions within the active circuit.

9-3 ELECTRICAL MEASUREMENTS.

All electrical measurements were made using a Tektronix 3260 test system. This is a computer-controlled test system that can make parametric and switching measurements on integrated circuits. A major feature of the machine is its built in graphics capability that enables the data for each device to be plotted on-line during testing. This allows the operator to quickly determine if valid data are obtained while the device is still in the test socket. Any devices with an abnormal response are immediately retested; the result is a much higher quality data base than that achieved with less interactive test instruments.

For circuit measurements, a special linear test fixture was used which provides the closed-loop conditions required for linear circuit testing. This test fixture is fully controlled by the 3260 test system, and can sequence through a series of measurements in 20 seconds, automatically recording the data.

Some special measurements were made in addition to the normally specified electrical parameters. These include the first-stage current I_1, which is of extreme importance in evaluating input degradation, and the output source and sink currents. The parameters measured for each device are listed in Table 9.

Common-emitter current gain (h_{FE}), forward base-emitter voltage (V_{BE}) and collector-base leakage current (I_{CBO}) were measured for each of the breakout transistors using the 3260 test system. These are the parameters that are most sensitive to radiation damage. On-line plots of h_{FE} vs. I_C were made during testing to detect abnormal behavior. Table 10 lists the electrical conditions used for gain measurements of the different transistor types.

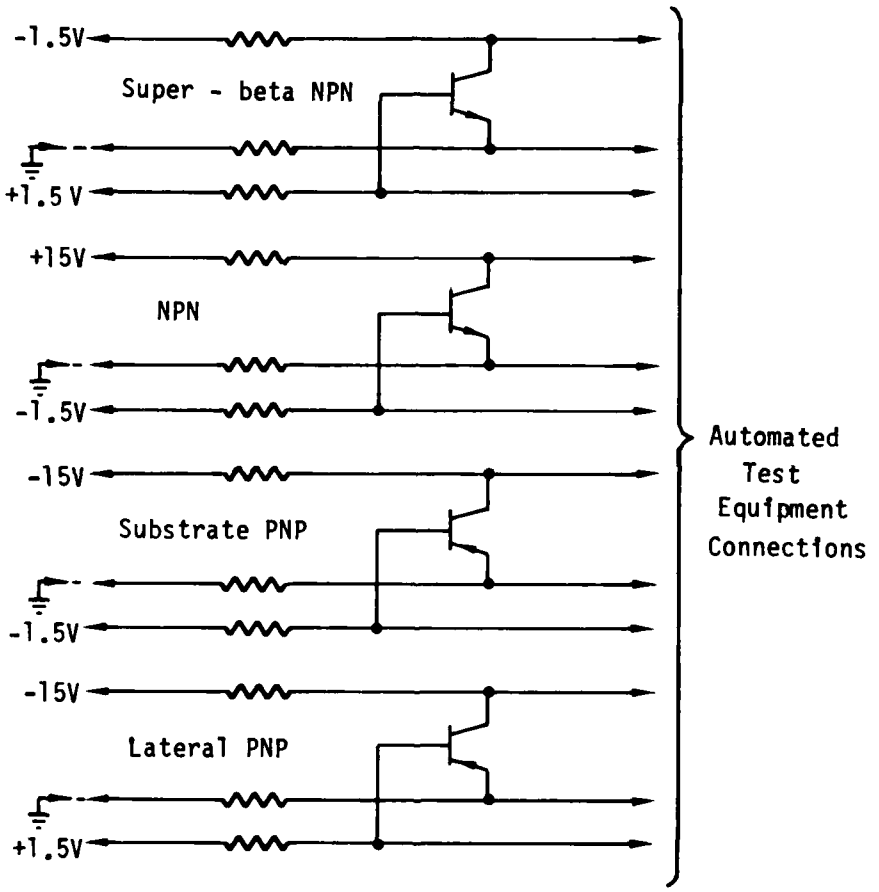


Figure 29. Electrical schematic of transistor test fixture.

Table 9. Electrical measurements for 108A circuits.

Test	Symbol	Test Conditions V_{CC} = +15V, V_{EE} = -15V
Input Offset Voltage	V_{OS}	
Input Bias Current	I_B	
Input Offset Current	I_{OS}	
Output Sink Current	I_{SINK}	V_{IN} = -1V, V_{OUT} = 0
Output Source Current	I_{SOURCE}	V_{IN} = +1V, V_{OUT} = 0
Positive Supply Current	I_{CC+}	
First-Stage Current Source	I_1	V_{COMP} = 15V, Measure I_{COMP}
Positive Slew Rate	+Slew Rate	Input = -5V to +5V Pulse Voltage Follower Configuration Measure 40% to 80% Slope
Negative Slew Rate	-Slew Rate	Input = +5V to -5V Pulse Voltage Follower Configuration Measure 40% to 80% Slope
Open-Loop Gain (Unloaded)	A_{OL} (Unloaded)	R_L = ∞
Open-Loop Gain (Loaded)	A_{OL} (Loaded)	R_L = 10 KΩ

Table 10. Electrical measurements for breakout transistors.

Transistor Type	Parameters Measured	Test Conditions
Lateral PNP	h_{FE}, V_{BE}	V_{CE} = -10V, I_C = 10 μA, 20 μA, 50 μA, 100 μA, 200 μA, 500 μA
	I_{CBO}	V_{CB} = -10V
Substrate PNP	h_{FE}, V_{BE}	V_{CE} = (-10V), I_C = 10 μA, 20 μA, 50 μA. 100 μA, 200 μA, 500 μA, 1 mA, 2 mA, 5 mA, 10 mA
	I_{CBO}	V_{CB} = (-10V)
NPN	h_{FE}, V_{BE}	V_{CE} = +10V, I_C = 10 μA, 20 μA, 50 μA, 100 μA, 200 μA, 500 μA, 1 mA, 2 mA, 5 mA, 10 mA
	I_{CBO}	V_{CB} = +10V
Super-β NPN	h_{FE}, V_{BE}	V_{CE} = +10V, I_C = 10 μA, 20 μA, 50 μA, 100 μA, 200 μA, 500 μA, 1 mA, 2 mA, 5 mA
	I_{CBO}	V_{CB} = +10V

SECTION 10

HARDNESS ASSURANCE APPLICATIONS

10-1 INTRODUCTION.

The results of this study are particularly useful for the planning and implementation of hardness assurance for linear integrated circuits. There are several basic questions that need to be answered before the optimum combination of hardness assurance methods can be selected. The most fundamental is that of device radiation response variability; this establishes the need for hardness assurance in terms of survivability and the margin between the mean response and the system radiation level. Other hardness assurance issues include the following:

1) Sampling methods.
2) Selection and interpretation of electrical parameters.
3) Use of test patterns.
4) Use of lower grade devices for lot sampling.
5) Electrical screens.
6) Effectiveness of controls at the manufacturing level.
7) Radiation testing methods.

10-2 APPLICATIONS OF RESULTS.

The circuit and breakout transistor test results show that most devices from either a wafer or diffusion lot have variations in damage factor of about a factor of 2. However, there are small numbers of devices with larger variability. At present, there is no way to eliminate these devices by screening, so that additional margin must be used in the system design. Based on these data, margins of a factor of 10 or more are needed to avoid statistical failures from these devices. These devices are discussed in more detail in Section 10-3.

The results of this study show that the optimum sampling level is the diffusion lot level. Only slight differences occurred in the hardness of wafers from a given diffusion lot. However, there is always the possibility that one wafer may be different because of contamination, variations in starting material, or processing variations. There were only eight wafers involved in this study. Furthermore, the difficulties of producing 108A devices with acceptable yield may result in less variation between wafers because of the extra attention paid to processing details. Hence, these results may not be typical of every linear device.

The close agreement between the breakout transistor and circuit results shows that breakout transistors may be used as suitable test patterns to evaluate diffusion lot hardness. It is important that irradiations are done in a forward-biased condition. Lower grade devices (such as 308A or 108 devices) may also be used for test patterns. This is extremely important for low-yield devices, because of the limited number of premium grade parts.

The 108A devices provided by AMD had relatively uniform electrical parameters. However, previous experience with other 108A devices has shown that some devices may have extreme values of first-stage current. Because this current source determines the internal margin of the input circuit, it is a valuable screening parameter for op-amps used in hardened systems.

Although no explicit controls were placed on the manufacturer, the variability of these three diffusion lots provides an estimate of the amount of variability to be expected with standard baseline control methods. These devices were fabricated over a four-month time period, and represent typical processing variations from this manufacturer.

The testing results for these devices show that substantial annealing did not occur over short time periods. Although all measurements were made quickly after irradiation, this was not necessary for these particular devices. The temperature coefficient of the input offset voltage increased after irradiation, which complicated the interpretation of offset voltage data. This must be considered when developing test methods for lot sample testing.

10-3 ABNORMAL DEVICES—THE "MAVERICK" PROBLEM.

Although this study was not intended to solve the difficult problem of identifying screening methods for devices with abnormally high radiation responses (so called "maverick" devices), the results of the study provide insight into the probable causes of such behavior. A logical first step in solving the "maverick" problem is the determination of the failure mechanisms for these abnormal devices. Once the mechanisms are known, hardness assurance methods can be developed to eliminate or control these devices.

Abnormal circuit responses could be caused by internal transistors that have unusually high radiation responses (transistor-related failure) or by circuit-related mechanisms, such as inadequate gain margins or high leakage currents that

cause the circuit to have increased radiation sensitivity, even though the radiation response of the internal transistors is well-behaved. The breakout transistor results can be used to estimate the relative importance of transistor-related failures. A total of 120 breakout transistor packages (three transistors per package) were irradiated from the eight wafers. Although some of the transistors had electrical abnormalities and were not irradiated*, none of the irradiated devices exhibited abnormal response. This bounds the failure rate, and, since this failure rate is much lower than that of the circuits, leads to the conclusion that the mechanisms for "maverick" behavior are connected with the circuit design, not the internal components.

The behavior of the circuits lends additional support to this conclusion. The offset voltage change of several of the abnormal circuits was initially negative, but became positive at higher total dose levels. Examples of this behavior are shown in Figures 15 and 16. Clearly there is an additional mechanism which changes the radiation response at low levels, and also increases the sensitivity of the circuit. If one or more of the internal transistors were abnormally sensitive to radiation, the abnormal radiation response would continue to dominate the circuit behavior unless the high response saturated at low total dose levels. Since no hint of such behavior was observed in the radiation tests of breakout transistors, the logical conclusion is that this response is due to leakage currents or low gain margins within the circuit.

There are several hardness assurance methods that could be useful in controlling such behavior. These include:

1) Electrical screens, perhaps comparing results at two or more temperatures.
2) Process controls to eliminate the mechanism.
3) Custom test points which allow direct determination of internal gain margins, and
4) Irradiate-anneal.

*The breakout transistors were not burned in, and were only tested at one operating condition by the manufacturer.

The x-y traceability results show that the radiation response of internal components are relatively uniform. The use of adjacent test patterns or test circuits would not be effective in controlling the "maverick" devices observed in this study because the mechanism is not abnormal sensitivity of local regions of a wafer, but isolated circuits which have internal defects. Subwafer traceability may be effective for other linear circuit processes, but it is not needed for 108A circuits from this manufacturer, which have adequate subwafer homogeneity in a radiation environment.

SECTION 11

CONCLUSIONS AND RECOMMENDATIONS

11-1 CONCLUSIONS.

Although this study was restricted to 108A-type operational amplifiers, many of the results can be applied to other linear circuits. The data on breakout transistor gain degradation show the importance of characterizing damage linearity for all types of internal transistors. The relative damage of these transistors may be different at different radiation levels because of damage saturation, which is extremely important when analyzing the mechanisms for degradation of linear integrated circuits. The analysis of the 108A circuit shows that several possible failure mechanisms do not occur because of saturation of substrate PNP damage at low levels, and also shows the importance of V_{BE}-I_C characteristics in typical linear integrated circuit designs.

The homogeneity data shows that device traceability must be maintained at least at the diffusion lot level, and that little advantage is gained by requiring higher levels of traceability for hardness assurance control.

Although this approach is effective in limiting the hardness variability of most devices, there are a small number of devices with abnormally high responses which are not effectively controlled by traditional hardness assurance methods. Comparing the breakout transistor and circuit results leads to the conclusion that this behavior is not caused by transistors with unusually high damage factors, but by high leakage currents or limited gain margin within the circuit. Similar results would be expected for other linear circuits which use active current sources and high gain in a single stage.

11-2 RECOMMENDATIONS.

Additional work needs to be done to determine the mechanisms for "maverick" behavior, since the mechanism must be established before effective hardness assurance controls can be developed. This is a major problem area for linear integrated circuits, and because of its random occurrence, cannot be solved by lot sampling or test pattern techniques.

The study also showed that potential failure mechanisms may occur which may not be detected by routine radiation testing. Careful analysis and understanding of the circuit requirements is a necessary complement to test data, and more effort needs to be spent in analyzing the response mechanisms of complex linear integrated circuits.

SECTION 12

REFERENCES

1. I. Arimura, et al., "A Study of Electronics Radiation Hardness Assurance Techniques: Vol. III," AFWL Technical Report AFWL-TR-73-134, Vol. III, Jan. 1974.

2. A. G. Stanley, et al., "Voyager Electronic Parts Radiation Program: Vol. II." JPL Technical Report 77-41, Vol. II, Dec. 1978.

3. L. J. Palkuti, L. L. Sivo and R. B. Greegor, IEEE Trans. Nucl. Sci., Vol. NS-23, No. 6, Dec. 1976.

4. A. G. Stanley and M. K. Gauthier, IEEE Trans. Nucl. Sci., Vol. NS-24, No. 6, Dec. 1977.

5. A. H. Johnston, IEEE Trans. Nucl. Sci., Vol. NS-23, No. 6, Dec. 1976.

APPENDIX A

SAMPLE ELECTRICAL DATA FOR 108-TYPE CIRCUITS

Sample data for 108-type circuits from the different wafers and diffusion lots are contained in this appendix. A sample of five devices was arbitrarily picked for each wafer. The most significant digit of the serial number indicates the electrical category of the circuit: 1 = 108A, 2 = 108, 3 = 308A, 4 = 308. Table A-1 below summarizes the radiation levels for each wafer.

Table A-1. Radiation levels for each wafer.

Lot	Wafer	Level 0	1	2	3	4	5	6	7
B	2*	pre-test	150 Krad	500 Krad	800 Krad	1.3 Mrad	2.0 Mrad	3.0 Mrad	<5.0 Mrad
	5	↓	↓	↓	↓	↓	↓	↓	4.4 Mrad
	6	↓	↓	↓	↓	↓	↓	↓	5.0 Mrad
	16	↓	↓	↓	↓	↓	↓	↓	↓
A	71	↓	↓	↓	↓	↓	↓	↓	↓
	76*	↓	↓	↓	↓	↓	↓	↓	↓
C	3	↓	↓	↓	↓	1.2 Mrad	1.8 Mrad	2.5 Mrad	—
	14	↓	↓	↓	↓	↓	↓	↓	—

*Wafers with x-y traceability.

The automated test equipment does not include the units of measurement. The units of measurement are V_{OS} (V), all currents (A), slew rate (V/μs), and gain (dimensionless). The suffixes used by the test system software printout have the following meanings: M = X 10^{-3}, U = X 10^{-6}, N = X 10^{-9}, P = X 10^{-12}.

Level 0

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	II
1709	200.5U	-62.50P	880.0P	355.0U	4.810U
1718	-27.65U	105.5P	870.0P	355.0U	5.215U
1720	-29.55U	41.50P	1.120N	340.0U	4.685U
1737	-125.0U	-22.00P	815.0P	340.0U	4.595U
1748	-85.50U	6.000P	845.0P	340.0U	4.395U
MEAN	-13.44U	13.70P	906.0P	346.0U	4.740U
STDDEV	126.4U	63.91P	122.2P	8.216U	305.6N

Wafer 5

2511	1.270M	24.50P	577.0P	315.0U	4.655U
2512	520.0U	57.00P	860.0P	365.0U	4.710U
2513	567.5U	61.00P	553.5P	320.0U	4.460U
2514	-805.0U	-63.00P	358.0P	320.0U	5.655U
2515	-1.450M	-59.00P	306.0P	295.0U	5.485U
MEAN	20.50U	4.100P	530.9P	323.0U	4.993U
STDDEV	1.113M	61.11P	218.8P	25.64U	538.2N

Wafer 6

1601	-420.5U	187.0P	1.245N	380.0U	4.910U
1602	119.0U	95.50P	980.0P	380.0U	4.900U
1603	-309.5U	-8.000P	634.0P	360.0U	5.540U
1604	22.45U	29.50P	790.0P	365.0U	4.990U
1606	-443.5U	23.50P	860.0P	335.0U	4.760U
MEAN	-206.4U	65.50P	901.8P	364.0U	5.024U
STDDEV	260.3U	77.66P	229.1P	18.51U	298.0N

Wafer 16

3911	229.5U	103.0P	1.005N	410.0U	4.020U
3912	-63.60U	-27.50P	1.130N	405.0U	4.365U
3913	-153.0U	378.5P	1.375N	420.0U	5.150U
3914	415.5U	80.50P	805.0P	405.0U	4.710U
3915	108.5U	51.50P	810.0P	400.0U	4.305U
MEAN	107.4U	117.2P	1.025N	408.0U	4.510U
STDDEV	227.4U	154.2P	239.0P	7.583U	433.8N

Level 0

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	-369.5U	-76.50P	1.160N	440.0U	4.675U
3212	-24.30U	-19.00P	1.375N	445.0U	4.775U
3213	128.0U	29.00P	960.0P	450.0U	3.805U
3214	38.75U	59.00P	865.0P	470.0U	3.600U
3215	-372.5U	-14.00P	1.335N	430.0U	4.590U
MEAN	-119.9U	-4.300P	1.143N	447.0U	4.289U
STDDEV	235.5U	51.57P	218.5P	14.83U	544.2N

Wafer 76

3052	192.0U	55.50P	750.0P	360.0U	3.940U
3055	-5.050U	71.50P	865.0P	370.0U	4.020U
3064	359.5U	104.5P	830.0P	380.0U	3.940U
3084	301.5U	48.00P	765.0P	375.0U	3.820U
3085	287.5U	48.00P	740.0P	370.0U	3.830U
MEAN	227.1U	65.50P	790.0P	371.0U	3.910U
STDDEV	143.0U	23.82P	54.66P	7.416U	84.26N

Lot C

Wafer 3

1301	-164.0U	66.00P	1.450N	425.0U	4.885U
1302	-5.400U	30.00P	1.400N	400.0U	5.135U
1303	-151.5U	-101.5P	1.160N	410.0U	5.155U
1304	-237.0U	41.00P	1.010N	430.0U	4.820U
1305	-201.5U	20.50P	1.205N	415.0U	5.060U
MEAN	-151.9U	11.20P	1.245N	416.0U	5.011U
STDDEV	88.47U	65.25P	180.3P	11.94U	150.7N

Wafer 14

3420	291.0U	158.5P	1.525N	490.0U	5.465U
3421	35.30U	-209.5P	3.550N	490.0U	4.700U
3422	113.0U	-90.50P	1.990N	460.0U	5.235U
3423	-150.5U	63.00P	1.370N	465.0U	5.550U
3424	77.00U	93.50P	2.420N	480.0U	5.440U
MEAN	73.16U	3.000P	2.171N	477.0U	5.278U
STDDEV	158.5U	149.9P	874.0P	13.96U	343.2N

Level 0

Lot B

Wafer 2

SN	AUL	AUL(L)	SR(+)	SR(-)	ISINK
1709	-116.4	114.7	70.06M	-83.67M	9.650M
1718	-123.1	111.4	75.00M	-88.87M	9.550M
1720	-123.9	111.2	68.08M	-81.51M	9.300M
1737	-115.5	116.1	70.01M	-84.10M	9.450M
1746	128.8	108.4	65.22M	-80.00M	9.300M
MEAN	-70.03	112.3	69.67M	-83.63M	9.450M
STDDEV	111.2	3.052	3.570M	3.367M	154.1U

Wafer 5

2511	-117.2	116.6	70.27M	-85.75M	9.400M
2512	-115.1	117.4	69.75M	-85.12M	9.400M
2513	-128.3	111.5	67.26M	-82.29M	9.250M
2514	118.6	106.4	94.24M	-113.4M	9.000M
2515	121.3	105.2	89.67M	-106.8M	8.950M
MEAN	-24.15	111.4	78.24M	-94.66M	9.200M
STDDEV	131.6	5.613	12.67M	14.32M	215.1U

Wafer 6

1601	132.3	109.0	71.17M	-85.44M	9.800M
1602	-115.6	115.5	75.84M	-89.87M	9.850M
1603	-116.2	118.6	85.33M	-101.8M	9.500M
1604	-111.7	126.8	79.27M	-95.13M	9.500M
1606	-117.3	114.4	70.27M	-83.79M	9.400M
MEAN	-65.70	116.9	76.38M	-91.20M	9.610M
STDDEV	110.7	6.562	6.190M	7.378M	201.2U

Wafer 16

3911	-122.8	111.0	55.90M	-66.97M	9.750M
3912	-136.1	108.7	63.06M	-76.74M	10.05M
3913	-103.5	-110.1	75.79M	-91.94M	9.300M
3914	111.2	104.2	71.44M	-88.82M	9.550M
3915	-121.4	110.7	62.14M	-76.41M	9.700M
MEAN	-74.52	64.90	65.66M	-80.17M	9.670M
STDDEV	104.5	97.88	7.913M	10.17M	275.2U

Level 0

Lot A

Wafer 71

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
3211	-134.1	108.4	64.72M	-78.06M	10.70M
3212	142.9	106.8	68.72M	-83.86M	10.65M
3213	139.0	107.4	49.38M	-60.33M	11.10M
3214	117.6	104.8	47.54M	-58.46M	11.35M
3215	123.6	108.6	63.29M	-77.78M	11.15M
MEAN	77.80	107.2	58.73M	-71.70M	10.99M
STDDEV	116.9	1.551	9.607M	11.51M	302.9U

Wafer 76

3052	-128.0	112.1	53.07M	-64.68M	10.45M
3055	-120.1	109.8	55.33M	-69.06M	10.10M
3064	-123.3	110.1	52.45M	-65.44M	10.35M
3084	-134.3	108.7	50.37M	-62.42M	10.30M
3085	-132.0	108.6	51.23M	-62.07M	10.25M
MEAN	-127.5	109.9	52.49M	-64.73M	10.29M
STDDEV	5.868	1.427	1.903M	2.815M	129.4U

Lot C

Wafer 3

1301	-118.6	111.2	76.54M	-95.67M	9.200M
1302	-113.0	116.9	84.09M	-104.0M	9.600M
1303	-122.7	110.6	82.61M	-104.0M	9.400M
1304	-119.3	112.1	80.21M	-98.51M	9.500M
1305	-117.7	115.2	83.26M	-102.8M	9.700M
MEAN	-118.3	113.2	81.34M	-101.0M	9.480M
STDDEV	3.492	2.757	3.049M	3.720M	192.4U

Wafer 14

3420	-114.6	115.7	89.41M	-109.7M	10.00M
3421	-115.1	116.1	70.78M	-88.66M	9.950M
3422	-117.1	117.2	83.96M	-103.6M	9.700M
3423	-115.9	114.7	89.41M	-109.1M	9.550M
3424	-117.8	113.2	66.75M	-106.5M	9.900M
MEAN	-116.1	115.4	84.06M	-103.5M	9.820M
STDDEV	1.340	1.499	7.762M	8.645M	189.1U

Level 1

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	II
1709	324.5U	657.5P	3.385N	345.0U	4.930U
1718	167.5U	660.0P	3.265N	345.0U	5.255U
1720	189.5U	154.5P	3.000N	350.0U	4.740U
1737	21.45U	524.0P	2.950N	335.0U	4.695U
1748	69.50U	391.0P	2.675N	325.0U	4.500U
MEAN	154.5U	477.4P	3.059N	340.0U	4.824U
STDDEV	117.5U	211.9P	282.9P	10.00U	285.3N

Wafer 5

2511	1.445M	159.5P	2.950N	305.0U	4.655U
2512	800.0U	74.00P	3.810N	350.0U	4.710U
2513	730.0U	-16.50P	2.345N	305.0U	4.505U
2514	-680.0U	-97.50P	1.935N	305.0U	5.690U
2515	-1.360M	-52.00P	1.770N	285.0U	5.520U
MEAN	167.0U	13.50P	2.562N	310.0U	5.016U
STDDEV	1.162M	103.1P	833.0P	23.98U	546.2N

Wafer 6

1601	-262.0U	357.0P	3.840N	370.0U	4.935U
1602	270.5U	-30.50P	3.105N	365.0U	4.975U
1603	-238.5U	-3.500P	2.280N	355.0U	5.670U
1604	134.0U	28.50P	2.515N	345.0U	5.130U
1606	-316.5U	-87.00P	2.680N	335.0U	4.840U
MEAN	-82.50U	52.90P	2.884N	354.0U	5.110U
STDDEV	265.9U	175.2P	613.5P	14.32U	330.1N

Wafer 16

3911	539.5U	-80.00P	2.270N	385.0U	4.070U
3912	339.5U	-10.50P	2.830N	390.0U	4.370U
3913	47.05U	404.5P	2.885N	405.0U	5.280U
3914	645.0U	28.50P	2.315N	400.0U	4.765U
3915	351.5U	75.00P	2.375N	395.0U	4.375U
MEAN	384.5U	83.50P	2.535N	395.0U	4.572U
STDDEV	228.5U	188.2P	297.4P	7.906U	466.4N

Level 1

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	-117.0U	4.075N	6.900N	425.0U	4.770U
3212	202.0U	4.190N	7.100N	425.0U	4.910U
3213	499.5U	-29.70N	4.040N	420.0U	3.865U
3214	485.5U	840.0P	3.115N	440.0U	3.605U
3215	-129.0U	2.740N	5.795N	405.0U	4.715U
MEAN	188.2U	-3.571N	5.390N	423.0U	4.373U
STDDEV	307.9U	14.67N	1.758N	12.55U	593.9N

Wafer 76

3052	537.5U	37.00P	2.165N	370.0U	3.860U
3055	342.0U	-33.00P	2.265N	355.0U	3.980U
3064	745.0U	-130.0P	2.025N	365.0U	3.890U
3084	476.0U	1.530N	2.000N	365.0U	3.830U
3085	638.0U	11.00P	2.030N	365.0U	3.780U
MEAN	547.7U	283.0P	2.097N	364.0U	3.868U
STDDEV	153.8U	700.0P	113.9P	5.477U	74.63N

Lot C

Wafer 3

1301	592.5U	1.865N	8.650N	400.0U	4.630U
1302	760.0U	3.920N	12.10N	385.0U	4.955U
1303	425.0U	3.360N	11.20N	380.0U	4.910U
1304	665.0U	1.680N	8.750N	405.0U	4.550U
1305	614.5U	2.770N	10.35N	390.0U	4.800U
MEAN	611.4U	2.719N	10.21N	392.0U	4.769U
STDDEV	122.5U	957.2P	1.511N	10.37U	175.2N

Wafer 14

3420	1.290M	4.830N	12.00N	455.0U	5.260U
3421	1.360M	3.245N	14.00N	465.0U	4.110U
3422	1.325M	5.085N	15.45N	420.0U	4.695U
3423	995.0U	6.365N	15.15N	430.0U	5.040U
3424	1.025M	4.780N	12.25N	450.0U	5.175U
MEAN	1.199M	4.861N	13.77N	444.0U	4.856U
STDDEV	174.6U	1.110N	1.599N	18.51U	469.4N

Level 1

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	148.4	106.2	70.85M	-85.44M	8.100M
1718	120.8	104.5	74.57M	-90.33M	8.000M
1720	120.7	104.7	66.74M	-81.73M	8.100M
1737	-128.6	107.2	70.27M	-84.60M	7.950M
1748	116.0	103.9	65.71M	-80.97M	7.850M
MEAN	75.48	105.3	69.63M	-84.61M	8.000M
STDDEV	114.8	1.346	3.538M	3.709M	106.1U

Wafer 5

2511	-130.6	108.2	68.92M	-83.98M	8.000M
2512	-136.2	106.3	70.03M	-85.33M	8.000M
2513	125.8	105.9	66.75M	-80.83M	7.900M
2514	113.8	103.0	93.89M	-112.2M	7.700M
2515	115.2	101.6	88.41M	-106.4M	7.750M
MEAN	17.59	105.0	77.60M	-93.75M	7.870M
STDDEV	137.9	2.660	12.58M	14.44M	139.6U

Wafer 6

1601	115.5	103.7	70.90M	-85.44M	8.200M
1602	-131.2	106.7	76.18M	-90.00M	8.100M
1603	-119.2	111.5	85.01M	-101.6M	8.050M
1604	-114.2	112.9	79.04M	-96.18M	8.000M
1606	-127.6	107.7	70.08M	-83.98M	7.950M
MEAN	-75.34	108.5	76.24M	-91.45M	8.060M
STDDEV	106.9	3.737	6.149M	7.422M	96.16U

Wafer 16

3911	116.6	103.1	55.33M	-67.76M	8.200M
3912	111.9	101.2	61.71M	-76.74M	8.450M
3913	-105.3	-138.8	77.20M	-93.75M	8.050M
3914	107.6	100.8	70.85M	-88.04M	8.150M
3915	119.3	103.5	61.48M	-75.74M	8.300M
MEAN	70.03	53.96	65.31M	-80.41M	8.230M
STDDEV	98.13	107.8	8.651M	10.38M	152.5U

Level 1

Lot A

Wafer 71

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
3211	116.2	103.1	64.49M	-79.25M	9.150M
3212	115.1	102.4	69.58M	-86.42M	9.100M
3213	111.9	101.5	50.20M	-63.76M	9.350M
3214	107.3	99.62	48.46M	-60.57M	9.550M
3215	112.7	103.8	64.74M	-80.68M	9.500M
MEAN	112.6	102.1	59.49M	-74.14M	9.330M
STDDEV	3.427	1.618	9.515M	11.31M	201.9U

Wafer 76

3052	113.8	103.8	50.90M	-64.96M	8.650M
3055	116.9	102.3	54.28M	-69.35M	8.450M
3064	114.6	102.3	51.82M	-65.69M	8.600M
3084	113.2	101.7	48.96M	-61.50M	8.600M
3085	113.5	102.0	49.29M	-62.39M	8.600M
MEAN	114.4	102.4	51.05M	-64.78M	8.580M
STDDEV	1.481	826.4M	2.151M	3.091M	75.83U

Lot C

Wafer 3

1301	104.2	96.51	70.30M	-88.27M	7.250M
1302	102.5	96.21	77.66M	-99.40M	7.750M
1303	102.3	96.19	75.14M	-96.83M	7.450M
1304	103.3	96.24	70.28M	-89.97M	7.400M
1305	104.8	98.14	75.10M	-95.84M	7.650M
MEAN	103.4	96.66	73.70M	-94.06M	7.500M
STDDEV	1.052	837.5M	3.276M	4.735M	200.0U

Wafer 14

3420	104.2	96.66	79.78M	-104.0M	7.850M
3421	101.1	94.47	59.41M	-78.56M	7.750M
3422	101.8	95.70	69.80M	-90.93M	7.250M
3423	105.5	96.23	76.85M	-99.10M	7.000M
3424	106.2	97.46	77.12M	-99.25M	7.750M
MEAN	103.7	96.10	72.59M	-94.36M	7.520M
STDDEV	2.214	1.117	8.245M	9.998M	373.5U

Level 2

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	I1
1709	566.0U	423.0P	6.450N	330.0U	4.860U
1718	470.0U	359.5P	6.330N	330.0U	5.155U
1720	484.5U	49.50P	6.260N	335.0U	4.710U
1737	266.5U	484.5P	5.860N	325.0U	4.665U
1748	313.0U	149.5P	5.325N	315.0U	4.445U
MEAN	420.0U	293.2P	6.045N	327.0U	4.767U
STDDEV	125.5U	185.7P	459.4P	7.583U	262.9N

Wafer 5

2511	1.670M	288.0P	5.240N	290.0U	4.610U
2512	1.190M	188.0P	6.450N	345.0U	4.720U
2513	1.040M	-149.5P	4.890N	290.0U	4.485U
2514	-475.5U	-92.00P	4.030N	305.0U	5.680U
2515	-1.115M	-93.50P	3.735N	280.0U	5.550U
MEAN	461.9U	28.20P	4.869N	302.0U	5.009U
STDDEV	1.193M	196.1P	1.076N	25.64U	561.3N

Wafer 6

1601	63.20U	1.090N	7.900N	355.0U	4.925U
1602	540.5U	-181.0P	6.750N	360.0U	4.940U
1603	1.650U	-65.50P	5.050N	340.0U	5.605U
1604	415.5U	-55.50P	5.525N	335.0U	5.115U
1606	-58.15U	-75.00P	5.800N	320.0U	4.845U
MEAN	192.5U	142.6P	6.205N	342.0U	5.086U
STDDEV	267.8U	532.0P	1.133N	16.05U	306.4N

Wafer 16

3911	780.0U	18.50P	5.075N	375.0U	4.035U
3912	740.0U	140.5P	5.955N	360.0U	4.275U
3913	295.5U	498.0P	5.530N	395.0U	5.275U
3914	1.030M	164.0P	5.180N	390.0U	4.710U
3915	634.5U	28.50P	5.290N	380.0U	4.365U
MEAN	696.0U	169.9P	5.406N	384.0U	4.532U
STDDEV	266.8U	194.6P	350.3P	8.216U	480.8N

Level 2

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	172.5U	4.160N	9.650N	405.0U	4.615U
3212	490.0U	3.385N	8.750N	415.0U	4.800U
3213	1.000M	278.0P	6.330N	420.0U	3.335U
3214	1.070M	650.0P	5.495N	425.0U	3.045U
3215	225.0U	2.425N	8.300N	410.0U	4.555U
MEAN	591.5U	2.180N	7.705N	415.0U	4.070U
STDDEV	423.1U	1.688N	1.732N	7.906U	814.9N

Wafer 76

3052	975.0U	-865.0P	4.520N	340.0U	3.435U
3055	750.0U	-690.0P	4.325N	345.0U	3.705U
3064	1.255M	-30.65N	4.365N	350.0U	3.390U
3084	1.085M	156.0P	4.250N	355.0U	3.435U
3085	1.070M	-88.00N	3.945N	360.0U	3.455U
MEAN	1.027M	-24.01N	4.281N	350.0U	3.484U
STDDEV	184.8U	38.09N	212.1P	7.906U	125.8N

Lot C

Wafer 3

1301	3.145M	-6.210N	20.10N	375.0U	3.680U
1302	2.660M	2.450N	24.75N	350.0U	4.045U
1303	1.955M	2.090N	25.10N	360.0U	4.065U
1304	3.290M	1.905N	21.85N	365.0U	3.500U
1305	2.690M	1.500N	22.65N	360.0U	4.070U
MEAN	2.748M	347.0P	22.89N	362.0U	3.872U
STDDEV	522.3U	3.681N	2.078N	9.083U	265.3N

Wafer 14

3420	3.955M	2.855N	24.05N	420.0U	4.500U
3421	4.445M	3.075N	29.00N	420.0U	2.220U
3422	4.030M	2.785N	30.00N	390.0U	4.030U
3423	3.815M	5.160N	31.90N	390.0U	4.170U
3424	3.685M	3.295N	23.75N	415.0U	4.445U
MEAN	3.986M	3.434N	27.74N	407.0U	3.873U
STDDEV	288.7U	985.4P	3.658N	15.65U	944.1N

Level 2

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	106.8	98.29	66.33M	-83.08M	6.850M
1718	105.4	97.26	71.44M	-86.29M	6.750M
1720	107.0	98.59	64.48M	-79.13M	7.050M
1737	110.1	99.64	67.53M	-82.29M	6.850M
1748	106.0	98.19	62.83M	-78.55M	6.800M
MEAN	107.0	98.39	66.92M	-81.86M	6.860M
STDDEV	1.820	856.3M	3.371M	3.152M	114.0U

Wafer 5

2511	115.1	101.8	65.74M	-81.37M	6.600M
2512	109.9	99.34	67.02M	-83.67M	6.900M
2513	110.3	99.38	64.24M	-79.48M	6.650M
2514	107.8	99.10	89.94M	-110.1M	6.600M
2515	106.7	97.18	84.80M	-102.7M	6.550M
MEAN	110.0	99.36	74.35M	-91.46M	6.660M
STDDEV	3.235	1.642	12.06M	13.95M	138.7U

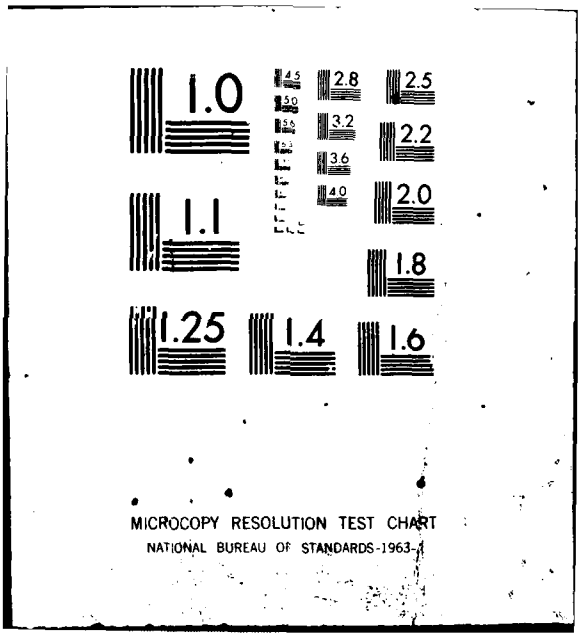
Wafer 6

1601	104.5	97.65	69.18M	-83.57M	7.100M
1602	115.8	100.4	72.75M	-87.39M	6.950M
1603	-117.5	108.3	82.24M	-100.1M	7.050M
1604	-117.1	107.0	76.29M	-92.90M	7.000M
1606	122.3	102.8	68.08M	-81.51M	6.950M
MEAN	21.60	103.2	73.71M	-89.09M	7.010M
STDDEV	126.9	4.460	5.756M	7.523M	65.19U

Wafer 16

3911	111.2	98.67	53.07M	-64.00M	7.050M
3912	102.5	95.10	58.14M	-73.26M	7.250M
3913	-106.3	112.8	73.89M	-92.06M	7.050M
3914	108.0	99.03	67.00M	-84.19M	7.000M
3915	109.4	98.49	59.54M	-73.22M	7.200M
MEAN	64.95	100.8	62.33M	-77.35M	7.110M
STDDEV	95.77	6.863	8.162M	10.90M	108.4U

AD-A084 645 BOEING CO SEATTLE WASH F/G 9/5
A TOTAL DOSE HOMOGENEITY STUDY OF THE 108A OPERATIONAL AMPLIFIE--ETC(U)
OCT 79 A H JOHNSTON, C A LANCASTER DNA001-78-C-0216
UNCLASSIFIED DNA-4977F NL


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Level 2

Lot A

Wafer 71

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
3211	111.1	99.48	62.09M	-77.15M	8.000M
3212	109.5	98.75	67.05M	-84.59M	8.050M
3213	106.6	97.45	46.92M	-60.13M	8.050M
3214	103.3	95.65	44.66M	-56.89M	8.250M
3215	107.6	100.1	61.91M	-78.75M	8.300M
MEAN	107.6	98.26	56.53M	-71.50M	8.130M
STDDEV	2.959	1.765	10.04M	12.23M	135.1U

Wafer 76

3052	105.9	98.76	47.38M	-60.86M	7.450M
3055	107.1	97.58	52.10M	-66.19M	7.350M
3064	104.9	96.67	47.87M	-61.95M	7.400M
3084	105.4	97.02	46.86M	-59.60M	7.450M
3085	106.0	97.33	46.64M	-59.19M	7.500M
MEAN	105.9	97.47	48.17M	-61.56M	7.430M
STDDEV	820.8M	798.9M	2.246M	2.807M	57.01U

Lot C

Wafer 3

1301	89.12	84.00	56.39M	-77.33M	5.400M
1302	88.17	83.82	64.45M	-86.03M	5.550M
1303	88.98	84.34	62.27M	-83.98M	5.350M
1304	88.66	83.61	54.86M	-76.07M	5.500M
1305	90.19	85.44	61.45M	-83.23M	5.600M
MEAN	89.02	84.24	59.89M	-81.33M	5.480M
STDDEV	746.3M	720.6M	4.067M	4.370M	103.7U

Wafer 14

3420	89.62	84.23	64.69M	-90.24M	4.500U
3421	87.96	82.78	40.13M	-63.78M	2.220U
3422	88.67	83.71	56.93M	-79.93M	4.030U
3423	89.97	83.49	61.41M	-86.97M	4.170U
3424	90.14	84.48	62.46M	-86.97M	4.445U
MEAN	89.27	83.74	57.13M	-81.58M	3.873U
STDDEV	927.0M	663.8M	9.911M	10.64M	944.1N

Level 3

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	I1
1709	810.0U	384.0P	8.750N	330.0U	4.760U
1716	725.0U	279.0P	8.200N	320.0U	5.035U
1720	715.0U	20.00P	8.500N	335.0U	4.580U
1737	482.5U	379.0P	7.650N	330.0U	4.575U
1746	527.0U	130.0P	7.050N	315.0U	4.305U
MEAN	651.9U	238.4P	8.030N	326.0U	4.651U
STDDEV	140.2U	159.7P	684.3P	8.216U	269.2N

Wafer 5

2511	1.870M	430.5P	7.250N	280.0U	4.520U
2512	1.520M	238.5P	9.000N	345.0U	4.585U
2513	1.330M	-100.5P	7.100N	300.0U	4.410U
2514	-303.0U	-173.0P	5.625N	295.0U	5.610U
2515	-900.0U	-174.0P	5.500N	290.0U	5.445U
MEAN	703.4U	44.30P	6.895N	302.0U	4.914U
STDDEV	1.225M	275.1P	1.428N	25.15U	566.5N

Wafer 6

1601	311.0U	1.430N	10.60N	345.0U	4.830U
1602	780.0U	-118.0P	9.500N	350.0U	4.860U
1603	157.0U	-19.00P	6.600N	335.0U	5.595U
1604	643.0U	-216.0P	7.400N	340.0U	5.040U
1606	178.0U	-194.5P	7.700N	320.0U	4.750U
MEAN	413.8U	176.5P	8.360N	338.0U	5.015U
STDDEV	282.3U	705.0P	1.641N	11.51U	341.1N

Wafer 16

3911	1.050M	61.50P	6.750N	375.0U	3.955U
3912	1.105M	88.00P	7.850N	375.0U	4.105U
3913	513.0U	591.0P	7.250N	395.0U	5.160U
3914	1.320M	181.0P	7.000N	375.0U	4.660U
3915	935.0U	93.00P	7.250N	370.0U	4.270U
MEAN	984.6U	202.9P	7.220N	378.0U	4.434U
STDDEV	298.4U	221.6P	408.7P	9.747U	493.0N

Level 3

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	362.5U	3.580N	10.60N	400.0U	4.410U
3212	655.0U	3.295N	10.20N	410.0U	4.680U
3213	1.345M	1.470N	7.900N	405.0U	2.670U
3214	1.490M	875.0P	6.850N	430.0U	2.495U
3215	457.0U	2.770N	10.50N	400.0U	4.380U
MEAN	861.9U	2.398N	9.210N	409.0U	3.767U
STDDEV	520.6U	1.175N	1.722N	12.45U	1.006U

Wafer 76

3052	1.345M	-260.0P	6.160N	340.0U	3.040U
3055	1.075M	-8.800N	5.670N	360.0U	3.375U
3064	1.665M	98.50P	5.720N	350.0U	3.045U
3084	1.460M	131.5P	5.590N	345.0U	3.030U
3085	1.405M	601.0P	5.345N	355.0U	3.105U
MEAN	1.390M	-1.646N	5.697N	350.0U	3.119U
STDDEV	213.3U	4.011N	296.2P	7.906U	146.1N

Lot C

Wafer 3

1301	4.515M	1.825N	26.70N	355.0U	3.020U
1302	3.945M	2.845N	32.10N	335.0U	3.325U
1303	3.080M	2.495N	33.00N	335.0U	3.305U
1304	4.990M	1.855N	27.80N	370.0U	2.670U
1305	4.095M	1.980N	29.60N	340.0U	3.505U
MEAN	4.125M	2.200N	29.84N	347.0U	3.205U
STDDEV	711.6U	450.3P	2.701N	15.25U	255.4N

Wafer 14

3420	5.765M	4.260N	33.25N	415.0U	4.050U
3421	6.465M	4.840N	38.30N	415.0U	1.555U
3422	5.710M	3.780N	39.10N	380.0U	3.645U
3423	5.495M	4.985N	40.40N	380.0U	3.675U
3424	5.495M	3.895N	32.45N	405.0U	3.985U
MEAN	5.786M	4.352N	36.70N	399.0U	3.382U
STDDEV	398.9U	543.9P	3.605N	17.82U	1.037U

Level 3

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	103.0	95.22	65.46M	-80.75M	6.300M
1718	101.5	94.29	68.59M	-83.98M	6.200M
1720	103.1	95.65	62.15M	-77.14M	6.450M
1737	105.5	96.73	64.97M	-79.93M	6.250M
1748	102.7	95.59	60.62M	-76.35M	6.250M
MEAN	103.2	95.49	64.36M	-79.63M	6.290M
STDDEV	1.479	879.5M	3.096M	3.050M	96.18U

Wafer 5

2511	107.7	98.22	64.00M	-79.70M	6.100M
2512	104.2	95.88	64.97M	-81.29M	6.400M
2513	104.8	96.05	62.07M	-77.82M	6.100M
2514	104.9	96.96	66.45M	-107.4M	6.100M
2515	103.5	94.91	81.66M	-101.2M	6.050M
MEAN	105.0	96.40	71.63M	-89.47M	6.150M
STDDEV	1.608	1.248	11.33M	13.74M	141.4U

Wafer 6

1601	100.8	94.76	66.24M	-80.68M	6.600M
1602	107.3	96.78	70.35M	-85.54M	6.350M
1603	-130.9	104.8	80.30M	-96.90M	6.550M
1604	-135.8	102.7	74.34M	-90.61M	6.450M
1606	111.3	99.27	65.23M	-80.23M	6.400M
MEAN	10.53	99.67	71.29M	-86.79M	6.470M
STDDEV	131.4	4.135	6.198M	7.050M	103.7U

Wafer 16

3911	105.0	95.50	51.43M	-63.07M	6.600M
3912	98.52	91.92	56.03M	-70.85M	6.700M
3913	-109.7	104.6	71.17M	-88.49M	6.600M
3914	105.2	96.37	64.73M	-82.37M	6.500M
3915	103.8	94.80	56.96M	-70.79M	6.650M
MEAN	60.56	96.65	60.06M	-75.11M	6.610M
STDDEV	95.21	4.771	7.835M	10.17M	74.16U

Level 3

Lot A

Wafer 71

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
3211	109.0	97.71	60.18M	-74.48M	7.500M
3212	107.0	96.97	64.24M	-81.81M	7.550M
3213	102.6	94.20	43.76M	-56.08M	7.400M
3214	99.92	92.75	40.87M	-53.70M	7.700M
3215	105.3	98.00	59.99M	-76.41M	7.700M
MEAN	104.8	95.93	53.81M	-68.49M	7.570M
STDDEV	3.588	2.324	10.68M	12.74M	130.4U

Wafer 76

3052	101.7	95.74	44.78M	-56.82M	6.950M
3055	102.6	94.44	49.20M	-63.07M	6.900M
3064	100.8	93.41	45.25M	-58.01M	6.850M
3084	101.3	93.79	44.15M	-56.87M	6.950M
3085	102.1	94.33	44.11M	-56.50M	6.950M
MEAN	101.7	94.34	45.50M	-58.25M	6.920M
STDDEV	676.0M	885.8M	2.124M	2.752M	44.72U

Lot C

Wafer 3

1301	86.29	80.61	48.99M	-70.30M	4.750M
1302	85.68	80.58	57.26M	-79.38M	4.800M
1303	86.44	81.09	55.26M	-77.71M	4.650M
1304	85.64	80.12	47.86M	-70.04M	4.850M
1305	87.14	81.84	54.53M	-77.33M	4.900M
MEAN	86.24	80.85	52.78M	-74.95M	4.790M
STDDEV	618.3M	653.5M	4.118M	4.435M	96.18U

Wafer 14

3420	86.10	80.41	57.94M	-84.65M	5.200M
3421	84.67	79.13	27.01M	-55.39M	5.500M
3422	85.48	80.03	50.45M	-75.78M	4.700M
3423	86.45	79.70	55.13M	-82.24M	4.350M
3424	86.49	80.47	55.52M	-82.08M	5.050M
MEAN	85.84	79.95	49.21M	-76.03M	4.960M
STDDEV	769.9M	552.9M	12.70M	12.00M	446.4U

Level 4

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	II
1709	1.150M	291.5P	11.65N	320.0U	4.635U
1718	1.090M	32.00P	10.75N	325.0U	4.870U
1720	1.095M	117.5P	11.35N	325.0U	4.405U
1737	810.0U	260.0P	10.25N	320.0U	4.350U
1748	850.0U	131.0P	9.650N	305.0U	4.030U
MEAN	999.0U	166.4P	10.73N	319.0U	4.458U
STDDEV	156.7U	107.4P	810.6P	8.216U	315.7N

Wafer 5

2511	2.145M	660.0P	10.20N	285.0U	4.390U
2512	1.940M	382.0P	12.45N	330.0U	4.470U
2513	1.720M	-166.0P	9.800N	280.0U	4.280U
2514	-109.5U	-145.5P	7.850N	285.0U	5.510U
2515	-617.5U	-112.5P	7.650N	265.0U	5.365U
MEAN	1.016M	123.2P	9.590N	289.0U	4.803U
STDDEV	1.281M	376.7P	1.961N	24.34U	585.4N

Wafer 6

1601	660.0U	1.875N	14.25N	335.0U	4.715U
1602	1.155M	-123.5P	12.35N	340.0U	4.735U
1603	378.0U	27.00P	9.200N	330.0U	5.440U
1604	965.0U	-277.5P	9.800N	330.0U	4.960U
1606	532.5U	-23.00P	10.65N	315.0U	4.605U
MEAN	738.1U	295.6P	11.25N	330.0U	4.891U
STDDEV	317.5U	890.5P	2.054N	9.354U	332.9N

Wafer 16

3911	1.570M	63.50P	9.350N	365.0U	3.740U
3912	1.655M	415.5P	10.90N	370.0U	3.885U
3913	805.0U	710.0P	9.700N	385.0U	5.095U
3914	1.705M	288.5P	9.750N	375.0U	4.565U
3915	1.370M	184.0P	10.15N	370.0U	4.110U
MEAN	1.421M	332.3P	9.970N	373.0U	4.279U
STDDEV	367.3U	247.9P	592.2P	7.583U	552.7N

Level 4

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	I1
3211	750.0U	3.590N	12.90N	395.0U	4.000U
3212	900.0U	3.045N	11.15N	405.0U	4.320U
3213	2.170M	1.230N	9.900N	395.0U	2.195U
3214	2.475M	1.130N	8.950N	425.0U	1.830U
3215	850.0U	2.355N	11.95N	400.0U	3.910U
MEAN	1.429M	2.270N	10.97N	404.0U	3.251U
STDDEV	824.5U	1.088N	1.577N	12.45U	1.148U

Wafer 76

3052	1.890M	-38.70N	8.100N	320.0U	2.565U
3055	1.650M	268.0P	7.750N	345.0U	2.850U
3064	2.270M	-51.45N	7.700N	340.0U	2.535U
3084	2.080M	195.5P	7.700N	345.0U	2.450U
3085	1.940M	-28.50N	7.200N	340.0U	2.530U
MEAN	1.966M	-23.64N	7.690N	338.0U	2.586U
STDDEV	230.1U	23.26N	320.9P	10.37U	153.6N

Lot C

Wafer 3

1301	5.900M	3.010N	32.40N	350.0U	2.405U
1302	5.370M	4.100N	39.35N	335.0U	2.675U
1303	4.350M	2.990N	39.00N	330.0U	2.675U
1304	6.665M	3.195N	34.00N	350.0U	2.320U
1305	5.470M	2.775N	35.50N	335.0U	2.955U
MEAN	5.551M	3.214N	36.05N	340.0U	2.606U
STDDEV	843.3U	517.2P	3.059N	9.354U	251.8N

Wafer 14

3420	7.715M	5.390N	41.00N	400.0U	3.600U
3421	8.945M	6.600N	46.25N	410.0U	1.085U
3422	7.570M	6.440N	49.00N	355.0U	3.235U
3423	7.355M	7.700N	50.80N	365.0U	3.190U
3424	7.395M	6.550N	40.60N	395.0U	3.535U
MEAN	7.796M	6.536N	45.57N	385.0U	2.929U
STDDEV	658.2U	818.8P	4.561N	23.72U	1.046U

Level 4

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	98.60	91.64	62.14M	-77.14M	5.550M
1718	97.81	91.10	64.97M	-80.75M	5.600M
1720	98.67	91.94	56.36M	-73.49M	5.800M
1737	100.4	92.79	61.27M	-76.74M	5.600M
1748	98.81	92.22	57.39M	-73.14M	5.600M
MEAN	98.86	91.94	60.82M	-76.25M	5.630M
STDDEV	954.4M	633.3M	3.041M	3.104M	97.47U

Wafer 5

2511	102.7	94.34	61.19M	-77.27M	5.400M
2512	99.25	91.87	60.74M	-78.72M	5.750M
2513	100.3	92.20	58.82M	-74.43M	5.300M
2514	101.5	94.01	83.10M	-103.3M	5.350M
2515	100.0	92.04	77.57M	-96.73M	5.250M
MEAN	100.7	92.89	68.28M	-86.08M	5.410M
STDDEV	1.356	1.183	11.21M	13.00M	198.1U

Wafer 6

1601	97.03	91.42	63.29M	-79.34M	5.900M
1602	100.9	92.28	67.01M	-82.37M	5.550M
1603	115.8	99.84	76.63M	-93.06M	5.900M
1604	110.9	97.99	70.61M	-86.63M	5.800M
1606	104.1	95.07	62.59M	-77.32M	5.700M
MEAN	105.7	95.32	68.03M	-83.74M	5.770M
STDDEV	7.588	3.606	5.782M	6.278M	148.3U

Wafer 16

3911	98.90	91.06	48.92M	-60.39M	5.950M
3912	94.52	88.41	52.90M	-67.79M	6.000M
3913	-129.0	98.54	67.53M	-84.71M	5.950M
3914	100.8	92.85	61.48M	-79.78M	5.800M
3915	98.65	90.92	54.42M	-68.63M	5.950M
MEAN	52.78	92.36	57.05M	-72.26M	5.930M
STDDEV	101.6	3.802	7.409M	9.815M	75.83U

Level 4

Lot A

Wafer 71

SN	AUL	AUL(L)	SR(+)	SR(-)	ISINK
3211	101.6	93.38	55.87M	-70.85M	6.850M
3212	101.6	93.36	60.39M	-77.84M	7.000M
3213	95.81	89.34	37.30M	-50.23M	6.850M
3214	93.94	88.16	33.16M	-47.43M	7.100M
3215	99.56	93.77	55.51M	-72.64M	7.150M
MEAN	98.51	91.60	48.45M	-63.80M	6.990M
STDDEV	3.486	2.641	12.30M	13.94M	138.7U

Wafer 76

3052	97.11	91.61	40.82M	-53.01M	6.350M
3055	97.52	90.59	45.15M	-58.78M	6.250M
3064	96.06	89.69	41.04M	-53.89M	6.250M
3084	96.38	89.95	39.44M	-52.08M	6.300M
3085	97.21	90.52	40.07M	-52.36M	6.350M
MEAN	96.86	90.47	41.30M	-54.02M	6.300M
STDDEV	609.4M	740.0M	2.240M	2.745M	50.00U

Lot C

Wafer 3

1301	84.14	77.97	42.18M	-64.00M	4.250M
1302	83.74	78.04	49.06M	-72.72M	4.200M
1303	84.55	78.60	47.82M	-70.84M	4.150M
1304	83.41	77.52	39.86M	-64.44M	4.400M
1305	84.86	79.03	46.63M	-71.97M	4.350M
MEAN	84.14	78.23	45.51M	-68.79M	4.270M
STDDEV	587.6M	587.0M	4.201M	4.229M	103.7U

Wafer 14

3420	83.34	77.26	51.45M	-79.86M	4.650M
3421	81.84	76.09	14.29M	-47.92M	5.000M
3422	82.88	77.08	45.24M	-72.03M	4.250M
3423	83.49	76.56	48.65M	-76.85M	3.950M
3424	83.63	77.40	49.78M	-77.50M	4.550M
MEAN	83.04	76.88	41.88M	-70.83M	4.480M
STDDEV	725.6M	542.5M	15.59M	13.12M	399.4U

Level 5

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	I1
1709	1.575M	312.5P	14.70N	310.0U	4.400U
1718	1.515M	215.5P	14.05N	310.0U	4.635U
1720	1.550M	105.0P	14.45N	330.0U	4.140U
1737	1.220M	367.5P	13.15N	300.0U	4.060U
1748	1.295M	70.00P	12.35N	295.0U	3.560U
MEAN	1.431M	214.1P	13.74N	309.0U	4.159U
STDDEV	162.0U	128.3P	974.9P	13.42U	404.2N

Wafer 5

2511	2.475M	920.0P	12.80N	280.0U	4.135U
2512	2.605M	660.0P	15.85N	325.0U	4.180U
2513	2.205M	-43.00P	12.40N	280.0U	4.120U
2514	145.5U	-52.00P	10.25N	280.0U	5.385U
2515	-311.5U	-78.50P	10.05N	265.0U	5.210U
MEAN	1.424M	281.3P	12.27N	286.0U	4.606U
STDDEV	1.392M	473.6P	2.352N	22.75U	634.7N

Wafer 6

1601	1.150M	2.360N	17.75N	325.0U	4.480U
1602	1.695M	11.00P	15.90N	330.0U	4.590U
1603	655.0U	59.50P	11.95N	320.0U	5.360U
1604	1.350M	-283.5P	12.50N	320.0U	4.820U
1606	980.0U	101.0P	13.65N	310.0U	4.400U
MEAN	1.166M	449.6P	14.35N	321.0U	4.730U
STDDEV	390.4U	1.079N	2.431N	7.416U	386.0N

Wafer 16

3911	2.470M	376.0P	12.20N	365.0U	3.310U
3912	2.540M	645.0P	13.95N	360.0U	3.490U
3913	1.280M	730.0P	12.20N	380.0U	4.875U
3914	2.300M	536.5P	12.60N	355.0U	4.275U
3915	2.415M	-1.860N	10.70N	365.0U	3.855U
MEAN	2.201M	85.50P	12.33N	365.0U	3.961U
STDDEV	522.3U	1.096N	1.161N	9.354U	630.6N

Level 5

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	1.240M	2.980N	14.40N	385.0U	3.525U
3212	1.520M	3.005N	14.30N	395.0U	3.875U
3213	3.125M	1.645N	12.35N	385.0U	1.720U
3214	3.670M	1.515N	11.60N	410.0U	1.320U
3215	1.500M	2.025N	14.80N	385.0U	3.420U
MEAN	2.211M	2.234N	13.49N	392.0U	2.772U
STDDEV	1.106M	717.4P	1.421N	10.95U	1.164U

Wafer 76

3052	2.610M	330.0P	10.60N	305.0U	2.085U
3055	2.420M	-62.10N	10.30N	325.0U	2.310U
3064	2.970M	316.5P	9.900N	335.0U	2.070U
3084	2.955M	512.0P	9.800N	335.0U	1.875U
3085	2.670M	845.0P	9.600N	335.0U	2.020U
MEAN	2.725M	-12.02N	10.04N	327.0U	2.072U
STDDEV	235.7U	28.00N	403.7P	13.04U	156.8N

Lot C

Wafer 3

1301	7.775M	4.690N	38.00N	335.0U	1.885U
1302	7.430M	6.300N	45.60N	320.0U	2.110U
1303	6.320M	4.670N	45.10N	330.0U	2.045U
1304	8.810M	5.095N	39.55N	340.0U	1.845U
1305	7.295M	4.965N	43.15N	325.0U	2.450U
MEAN	7.526M	5.144N	42.28N	330.0U	2.067U
STDDEV	898.3U	671.1P	3.373N	7.906U	240.5N

Wafer 14

3420	10.20M	8.450N	50.00N	390.0U	2.990U
3421	12.05M	11.20N	55.40N	410.0U	795.0N
3422	9.530M	8.650N	56.50N	360.0U	2.820U
3423	9.440M	10.15N	59.20N	360.0U	2.715U
3424	9.785M	8.400N	47.85N	380.0U	3.025U
MEAN	10.20M	9.370N	53.79N	380.0U	2.469U
STDDEV	1.075M	1.251N	4.713N	21.21U	944.3N

Level 5

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	94.59	88.15	58.94M	-73.85M	4.900M
1718	93.97	87.75	61.49M	-77.14M	5.000M
1720	94.61	88.34	54.80M	-69.10M	5.100M
1737	96.03	89.12	57.20M	-72.30M	4.950M
1748	94.79	88.60	52.61M	-68.02M	4.950M
MEAN	94.80	88.39	57.01M	-72.08M	4.980M
STDDEV	754.2M	510.3M	3.465M	3.681M	75.83U

Wafer 5

2511	98.59	90.98	56.32M	-71.93M	4.850M
2512	94.55	87.85	54.92M	-72.38M	5.100M
2513	96.22	88.54	54.35M	-69.36M	4.650M
2514	98.41	91.10	77.76M	-98.26M	4.750M
2515	97.13	89.39	72.44M	-92.87M	4.650M
MEAN	96.98	89.57	63.16M	-80.96M	4.800M
STDDEV	1.668	1.446	11.09M	13.52M	167.1U

Wafer 6

1601	93.85	86.36	59.33M	-74.90M	5.250M
1602	95.72	88.13	61.91M	-77.32M	4.850M
1603	105.3	95.55	72.71M	-89.20M	5.250M
1604	102.3	93.34	66.22M	-82.46M	5.150M
1606	98.52	90.98	57.95M	-73.26M	5.050M
MEAN	99.13	91.27	63.63M	-79.43M	5.110M
STDDEV	4.675	3.202	5.979M	6.476M	167.3U

Wafer 16

3911	93.14	86.49	44.22M	-56.24M	5.350M
3912	90.86	84.87	48.27M	-63.53M	5.400M
3913	104.3	92.27	61.48M	-79.27M	5.300M
3914	95.20	88.52	56.24M	-74.53M	5.200M
3915	93.35	86.58	49.20M	-63.29M	5.350M
MEAN	95.38	87.75	51.88M	-67.37M	5.320M
STDDEV	5.239	2.842	6.892M	9.329M	75.83U

Level 5

Lot A

Wafer 71

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
3211	96.58	89.63	51.55M	-65.73M	6.300M
3212	96.82	89.81	55.87M	-73.22M	6.350M
3213	91.16	85.40	29.16M	-44.20M	6.200M
3214	89.53	84.12	24.27M	-40.00M	6.500M
3215	95.26	89.97	50.97M	-67.54M	6.550M
MEAN	93.87	87.79	42.36M	-58.14M	6.380M
STDDEV	3.323	2.800	14.51M	14.97M	144.0U

Wafer 76

3052	92.84	87.77	35.71M	-48.31M	5.700M
3055	92.81	86.73	39.91M	-53.33M	5.650M
3064	91.98	86.22	36.07M	-49.66M	5.650M
3084	91.83	86.12	32.52M	-46.31M	5.700M
3085	92.76	86.85	34.29M	-47.56M	5.700M
MEAN	92.44	86.74	35.70M	-49.03M	5.680M
STDDEV	497.7M	657.1M	2.738M	2.692M	27.39U

Lot C

Wafer 3

1301	82.27	75.53	32.18M	-57.86M	3.850M
1302	82.15	75.53	37.58M	-64.89M	3.800M
1303	82.85	76.23	36.00M	-63.56M	3.750M
1304	81.28	74.86	30.41M	-57.30M	4.050M
1305	82.71	76.35	40.18M	-65.81M	3.900M
MEAN	82.25	75.70	35.27M	-61.89M	3.870M
STDDEV	616.1M	603.2M	3.974M	4.014M	115.1U

Wafer 14

3420	80.46	74.04	43.01M	-72.85M	4.200M
3421	78.76	72.88	3.117M	-39.54M	4.650M
3422	80.55	74.36	39.53M	-68.03M	3.900M
3423	80.77	73.61	40.77M	-71.17M	3.650M
3424	80.82	74.31	42.04M	-71.17M	4.150M
MEAN	80.27	73.84	33.69M	-64.55M	4.110M
STDDEV	858.3M	612.0M	17.14M	14.09M	373.2U

Level 6

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	I1
1709	2.205M	432.0P	17.40N	310.0U	4.010U
1718	2.165M	440.5P	16.75N	305.0U	4.220U
1720	2.290M	472.0P	17.70N	315.0U	3.710U
1737	1.855M	670.0P	16.05N	295.0U	3.620U
1748	1.915M	71.50P	14.80N	295.0U	2.915U
MEAN	2.086M	417.2P	16.54N	304.0U	3.695U
STDDEV	190.1U	216.3P	1.162N	8.944U	497.3N

Wafer 5

2511	2.945M	1.145N	15.80N	270.0U	3.820U
2512	3.525M	1.045N	19.50N	320.0U	3.860U
2513	2.855M	164.5P	15.45N	265.0U	3.880U
2514	520.5U	-82.00P	12.60N	275.0U	5.225U
2515	53.05U	-393.5P	12.60N	255.0U	5.070U
MEAN	1.980M	375.8P	15.19N	277.0U	4.371U
STDDEV	1.575M	686.6P	2.847N	25.15U	711.3N

Wafer 6

1601	1.910M	3.230N	21.85N	335.0U	4.065U
1602	2.580M	502.0P	20.00N	320.0U	4.315U
1603	1.075M	253.0P	14.85N	315.0U	5.110U
1604	1.895M	-238.0P	15.95N	315.0U	4.560U
1606	1.590M	338.0P	16.95N	300.0U	4.135U
MEAN	1.810M	817.0P	17.92N	317.0U	4.437U
STDDEV	547.4U	1.377N	2.916N	12.55U	422.1N

Wafer 16

3911	3.560M	905.0P	15.30N	345.0U	2.835U
3912	3.635M	1.045N	17.65N	350.0U	2.910U
3913	1.980M	995.0P	15.30N	380.0U	4.675U
3914	3.120M	745.0P	15.75N	355.0U	4.105U
3915	3.215M	670.0P	16.30N	360.0U	3.545U
MEAN	3.102M	872.0P	16.06N	358.0U	3.614U
STDDEV	664.4U	160.5P	979.4P	13.51U	786.5N

Level 6

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	2.080M	2.945N	16.90N	385.0U	2.885U
3212	2.355M	2.000N	17.70N	390.0U	3.295U
3213	4.790M	572.0P	14.75N	385.0U	1.145U
3214	3.685M	15.10N	14.65N	405.0U	925.0N
3215	2.395M	2.330N	17.45N	385.0U	2.840U
MEAN	3.061M	4.589N	16.29N	390.0U	2.218U
STDDEV	1.149M	5.940N	1.480N	8.660U	1.097U

Wafer 76

3052	3.780M	980.0P	13.65N	310.0U	1.590U
3055	3.570M	-14.60N	13.00N	330.0U	1.715U
3064	4.220M	-22.60N	12.50N	330.0U	1.480U
3084	4.400M	900.0P	12.45N	330.0U	1.265U
3085	3.985M	1.055N	12.10N	325.0U	1.345U
MEAN	3.991M	-6.853N	12.74N	325.0U	1.479U
STDDEV	332.2U	11.09N	601.5P	8.660U	181.5N

Lot C

Wafer 3

1301	9.530M	6.380N	44.05N	335.0U	1.560U
1302	9.115M	7.950N	52.05N	315.0U	1.700U
1303	7.920M	6.700N	52.35N	310.0U	1.695U
1304	10.70M	6.650N	45.70N	335.0U	1.490U
1305	8.980M	6.550N	46.75N	320.0U	2.015U
MEAN	9.249M	6.886N	48.58N	323.0U	1.692U
STDDEV	1.005M	619.9P	3.711N	11.51U	201.6N

Wafer 14

3420	12.40M	11.35N	57.15N	380.0U	2.580U
3421	11.15M	11.05N	64.05N	355.0U	2.500U
3422	11.40M	10.85N	61.90N	360.0U	2.530U
3423	11.35M	12.50N	66.60N	360.0U	2.360U
3424	11.95M	10.15N	53.95N	380.0U	2.565U
MEAN	11.65M	11.18N	60.73N	367.0U	2.507U
STDDEV	513.6U	859.9P	5.139N	12.04U	87.86N

Level 6

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	90.87	84.68	53.30M	-68.59M	4.350M
1718	90.66	84.55	55.72M	-71.44M	4.500M
1720	90.60	84.52	49.57M	-64.00M	4.500M
1737	92.13	85.43	52.01M	-66.22M	4.350M
1748	91.08	85.06	46.86M	-61.29M	4.350M
MEAN	91.07	84.85	51.49M	-66.31M	4.410M
STDDEV	622.3M	389.5M	3.409M	3.939M	82.16U

Wafer 5

2511	94.33	87.31	51.64M	-67.11M	4.300M
2512	90.11	83.73	50.41M	-67.98M	4.500M
2513	92.31	84.77	49.86M	-65.51M	4.000M
2514	95.06	87.93	72.59M	-92.99M	4.100M
2515	94.14	86.51	67.95M	-88.04M	4.050M
MEAN	93.19	86.05	58.49M	-76.33M	4.190M
STDDEV	1.996	1.758	10.90M	13.10M	207.4U

Wafer 6

1601	90.27	84.80	53.94M	-69.68M	4.700M
1602	90.67	83.77	56.05M	-72.03M	4.300M
1603	99.17	91.14	67.00M	-83.88M	4.700M
1604	96.09	88.83	61.48M	-77.90M	4.600M
1606	93.76	86.95	52.78M	-67.79M	4.500M
MEAN	93.99	87.10	58.25M	-74.26M	4.560M
STDDEV	3.747	2.987	5.924M	6.588M	167.3U

Wafer 16

3911	88.25	82.06	39.02M	-51.39M	4.700M
3912	86.62	80.84	42.90M	-57.93M	4.750M
3913	96.01	87.20	56.77M	-73.61M	4.650M
3914	90.85	84.53	51.78M	-69.70M	4.600M
3915	88.56	82.28	44.73M	-58.52M	4.700M
MEAN	90.06	83.38	47.04M	-62.23M	4.680M
STDDEV	3.651	2.518	7.140M	9.154M	57.01U

Level 6

Lot A

Wafer 71

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
3211	91.75	85.64	44.99M	-59.16M	5.750M
3212	92.01	85.85	50.08M	-66.57M	5.800M
3213	86.34	81.21	19.71M	-35.54M	5.700M
3214	84.76	79.83	15.55M	-33.41M	5.900M
3215	90.61	85.87	45.41M	-61.18M	5.950M
MEAN	89.10	83.68	35.15M	-51.17M	5.820M
STDDEV	3.325	2.926	16.18M	15.50M	103.7U

Wafer 76

3052	88.25	83.61	27.78M	-43.86M	5.200M
3055	88.33	82.64	31.29M	-46.61M	5.100M
3064	87.54	82.10	26.55M	-41.89M	5.100M
3084	87.15	81.76	22.09M	-37.24M	5.150M
3085	87.97	82.41	24.37M	-38.33M	5.150M
MEAN	87.85	82.50	26.42M	-41.59M	5.140M
STDDEV	497.9M	703.8M	3.484M	3.873M	41.83U

Lot C

Wafer 3

1301	80.16	73.19	23.96M	-51.06M	3.550M
1302	80.00	73.11	26.12M	-58.75M	3.500M
1303	80.78	73.85	27.17M	-56.61M	3.500M
1304	79.07	72.49	22.54M	-52.10M	3.750M
1305	80.64	73.90	32.92M	-60.47M	3.600M
MEAN	80.13	73.31	26.94M	-55.80M	3.580M
STDDEV	674.9M	585.1M	4.046M	4.102M	103.7U

Wafer 14

3420	78.13	71.63	35.94M	-68.24M	3.850M
3421	78.47	72.19	34.02M	-64.00M	3.700M
3422	78.33	72.25	33.09M	-64.00M	3.800M
3423	78.34	71.31	33.37M	-66.06M	3.450M
3424	78.30	71.75	34.89M	-65.82M	3.650M
MEAN	78.32	71.83	34.26M	-65.62M	3.730M
STDDEV	122.2M	394.7M	1.166M	1.755M	166.1U

Level 7

Lot B

Wafer 2

SN	VOS	IOS	IB	ICC	I1
1709	3.675M	1.280N	21.85N	310.0U	3.305U
1718	3.540M	995.0P	20.65N	300.0U	3.445U
1720	3.945M	1.335N	22.00N	310.0U	2.820U
1737	3.205M	1.215N	19.90N	290.0U	2.700U
1748	3.295M	633.5P	18.75N	265.0U	1.905U
MEAN	3.532M	1.092N	20.63N	299.0U	2.835U
STDDEV	297.6U	286.9P	1.363N	11.40U	607.5N

Wafer 5

1601	3.600M	4.510N	26.50N	325.0U	3.235U
1602	4.550M	1.875N	25.10N	320.0U	3.795U
1603	1.840M	900.0P	19.50N	310.0U	4.740U
1604	3.045M	440.5P	19.85N	310.0U	4.085U
1606	2.820M	1.255N	21.90N	300.0U	3.395U
MEAN	3.171M	1.796N	22.57N	313.0U	3.850U
STDDEV	999.5U	1.605N	3.127N	9.747U	599.1N

Wafer 6

2511	3.580M	1.630N	18.40N	270.0U	3.340U
2512	4.825M	1.780N	22.80N	315.0U	3.345U
2513	3.670M	342.0P	17.65N	260.0U	3.575U
2514	965.0U	169.5P	14.70N	270.0U	5.085U
2515	278.0U	55.00P	14.50N	245.0U	4.900U
MEAN	2.664M	795.3P	17.61N	272.0U	4.049U
STDDEV	1.943M	838.4P	3.380N	26.12U	869.0N

Wafer 16

3911	6.570M	2.225N	19.60N	345.0U	1.755U
3912	6.255M	2.395N	22.75N	345.0U	1.915U
3913	3.495M	1.680N	19.65N	360.0U	4.310U
3914	4.830M	1.650N	19.80N	345.0U	3.560U
3915	5.555M	2.165N	20.90N	360.0U	2.885U
MEAN	5.341M	2.023N	20.54N	351.0U	2.885U
STDDEV	1.231M	337.7P	1.345N	8.216U	1.084U

Level 7

Lot A

Wafer 71

SN	VOS	IOS	IB	ICC	II
3211	4.060M	3.655N	20.35N	375.0U	1.935U
3212	4.100M	3.835N	20.35N	385.0U	2.275U
3213	8.385M	3.565N	18.65N	380.0U	645.0N
3214	10.20M	3.890N	17.80N	400.0U	450.0N
3215	4.515M	3.165N	21.05N	380.0U	1.800U
MEAN	6.252M	3.622N	19.64N	384.0U	1.421U
STDDEV	2.854M	287.4P	1.357N	9.618U	818.9N

Wafer 76

3052	6.410M	1.925N	18.10N	300.0U	810.0N
3055	6.565M	-3.625N	17.30N	320.0U	890.0N
3064	5.355M	-33.90N	22.30N	325.0U	810.0N
3084	7.460M	6.500N	16.00N	320.0U	625.0N
3085	7.080M	-65.90N	16.10N	320.0U	700.0N
MEAN	6.574M	-19.00N	17.96N	317.0U	767.0N
STDDEV	799.1U	30.60N	2.578N	9.747U	104.3N

Level 7

Lot B

Wafer 2

SN	AOL	AOL(L)	SR(+)	SR(-)	ISINK
1709	86.09	79.96	44.39M	-59.16M	3.850M
1718	85.94	80.05	46.72M	-61.71M	4.050M
1720	85.30	79.41	40.52M	-54.34M	4.000M
1737	86.65	80.38	42.20M	-55.74M	3.850M
1748	86.15	80.25	34.32M	-49.09M	3.900M
MEAN	86.03	80.01	41.63M	-56.01M	3.930M
STDDEV	485.4M	373.4M	4.703M	4.825M	90.83U

Wafer 5

2511	90.86	83.91	46.96M	-61.17M	3.850M
2512	85.81	79.61	44.28M	-61.38M	4.000M
2513	88.63	81.15	45.04M	-60.73M	3.450M
2514	92.22	84.95	67.10M	-86.67M	3.600M
2515	91.22	83.79	63.50M	-82.65M	3.550M
MEAN	89.75	82.68	53.38M	-70.52M	3.690M
STDDEV	2.562	2.216	11.00M	12.99M	227.5U

Wafer 6

1601	84.83	79.45	43.59M	-58.54M	4.200M
1602	84.14	77.83	46.21M	-61.70M	3.650M
1603	92.57	85.69	57.56M	-73.89M	4.050M
1604	89.20	82.92	51.59M	-67.79M	4.000M
1606	88.01	81.47	44.11M	-59.16M	3.850M
MEAN	87.75	81.47	48.61M	-64.22M	3.950M
STDDEV	3.427	3.050	5.919M	6.528M	209.2U

Wafer 16

3911	80.95	75.43	26.05M	-40.65M	3.950M
3912	80.76	75.22	29.89M	-46.74M	4.050M
3913	87.27	80.39	48.41M	-65.46M	3.900M
3914	84.55	78.71	43.74M	-61.28M	3.850M
3915	82.13	76.31	36.30M	-50.46M	3.950M
MEAN	83.13	77.21	36.88M	-52.92M	3.940M
STDDEV	2.761	2.254	9.306M	10.27M	74.16U

Level 7

Lot A

Wafer 71

SN	AUL	AUL(L)	SR(+)	SR(-)	ISINK
3211	85.11	79.69	31.64M	-47.69M	5.050M
3212	85.74	80.21	37.90M	-54.11M	5.100M
3213	79.82	75.05	3.291M	-21.97M	5.050M
3214	77.89	73.39	608.0M	-19.38M	5.250M
3215	84.36	79.88	30.38M	-47.78M	5.300M
MEAN	82.58	77.65	142.2M	-38.19M	5.150M
STDDEV	3.506	3.168	260.7M	16.22M	117.3U

Wafer 76

3052	81.91	77.45	12.80M	-28.03M	4.550M
3055	81.42	76.30	14.61M	-32.41M	4.450M
3064	80.77	75.93	11.79M	-28.66M	4.550M
3084	79.98	75.13	7.642M	-22.29M	4.500M
3085	81.03	76.06	9.702M	-24.37M	4.500M
MEAN	81.02	76.18	11.31M	-27.15M	4.510M
STDDEV	723.2M	838.1M	2.710M	3.942M	41.83U

DISTRIBUTION LIST

DEPARTMENT OF DEFENSE

Assistant to the Secretary of Defense
Atomic Energy
ATTN: Executive Assistant

Command & Control Technical Center
Department of Defense
ATTN: C-362, G. Adkins

Defense Electronic Supply Center
ATTN: DESC-ECS, D. Hill
ATTN: DESC-ECS, J. Dennis
ATTN: DESC-ECS, J. Counsil
ATTN: DESC-EQM, R. Grillmeier
ATTN: DESC-ECT, J. Niles
ATTN: DESC-ECT, D. Droege
ATTN: DESC-ECP, B. Nunke

Defense Logistics Agency
ATTN: DLA-SE
ATTN: DLA-QEL, J. Slattery

Defense Material Specifications & Standard Office
ATTN: L. Fox

Defense Nuclear Agency
ATTN: RAEV, M. Kemp
ATTN: DDST
ATTN: RAAE, H. Fitz, Jr.
4 cy ATTN: TITL

Defense Supply Agency
ATTN: DSAH/SE 4A586

Defense Technical Information Center
12 cy ATTN: DD

Field Command
Defense Nuclear Agency
ATTN: FCPR

Field Command
Defense Nuclear Agency
Livermore Division
ATTN: FCPRL

National Security Agency
ATTN: T. Brown
ATTN: G. Daily

Undersecretary of Def. for Rsch. & Engrg.
ATTN: Strategic & Space Systems (OS)

DEPARTMENT OF THE ARMY

Aberdeen Proving Ground
Department of the Army
ATTN: S. Harrison

BMD Advanced Technology Center
Department of the Army
ATTN: ATC-T

BMD Systems Command
Department of the Army
ATTN: BMDSC-HW, R. Dekalb

DEPARTMENT OF THE ARMY (Continued)

Deputy Chief of Staff for Rsch. Dev. & Acq.
Department of the Army
ATTN: G. Ogden

Harry Diamond Laboratories
Department of the Army
ATTN: DELHD-N-RBH, J. Halpin
ATTN: DELHD-N-RBH, H. Eisen
ATTN: DELHD-N-RBC, J. McGarrity
ATTN: DELHD-N-P, F. Balicki

U.S. Army Armament Research & Development Command
ATTN: DRDAR-LOA-PD

U.S. Army Communications R&D Command
ATTN: D. Huewe

U.S. Army Missile R&D Command
ATTN: RSIC

U.S. Army Nuclear & Chemical Agency
ATTN: Library for A. Lind
ATTN: Library for A. Lowrey

White Sands Missile Range
Department of the Army
ATTN: STEWS-TE-AN, M. Squires
ATTN: STEWS-TE-AN, T. Leura
ATTN: STEWS-TE-AN, L. Meason
ATTN: STEWS-TE-NT, R. Williams

DEPARTMENT OF THE NAVY

Naval Air Systems Command
ATTN: AIR 350F

Naval Electronic Systems Command
ATTN: Code 5045.11, C. Suman

Naval Ocean Systems Center
ATTN: Code 4471

Naval Postgraduate School
ATTN: Code 1424

Naval Research Laboratory
ATTN: Code 5210, J. Davey
ATTN: Code 6601, E. Wolicki
ATTN: Code 6600, J. McEllinney
ATTN: Code 6701, J. Brown
ATTN: Code 5216, H. Hughes
ATTN: Code 6627, C. Guenzer
ATTN: Code 6650, A. Namenson

Naval Sea Systems Command
ATTN: SEA-06J, R. Lane

Naval Ship Engineering Center
ATTN: Code 6174D2

Naval Surface Weapons Center
ATTN: Code F31
ATTN: J. Downs
ATTN: R. Jenkins
ATTN: R. Smith

DEPARTMENT OF THE NAVY (Continued)

Naval Weapons Center
ATTN: Code 233

Naval Weapons Evaluation Facility
ATTN: Code AT-6

Naval Weapons Support Center
ATTN: Code 70242, J. Munarin
ATTN: Code 7024, T. Ellis
ATTN: Code 7024, J. Ramsey

Office of Naval Research
ATTN: Code 427, L. Cooper

Office of the Chief of Naval Operations
ATTN: OP 985F

Strategic Systems Project Office
Department of the Navy
ATTN: NSP-230, D. Gold
ATTN: NSP-2015
ATTN: NSP-2701, J. Pitsenberger
ATTN: NSP-27331, P. Spector

DEPARTMENT OF THE AIR FORCE

Air Force Aero-Propulsion Laboratory
ATTN: POD, P. Stover

Air Force Avionics Laboratory
ATTN: TEA, R. Conklin
ATTN: DHE

Air Force Institute of Technology
Air University
ATTN: ENP, J. Bridgeman

Air Force Materials Laboratory
ATTN: LTE

Headquarters
Air Force Systems Command
ATTN: DLCAM, T. Seale
ATTN: DLCA
ATTN: XRLA, R. Stead

Air Force Technical Applications Center
ATTN: TAE

Air Force Weapons Laboratory
Air Force Systems Command
ATTN: ELP, M. Knoll
ATTN: ELT, J. Ferry
ATTN: ELP, R. Maier
ATTN: ELP, G. Chapman
ATTN: SUL
ATTN: ELP, J. Mullis
ATTN: ELP, A. Loggins

Air Logistics Command
Department of the Air Force
ATTN: OO-ALC/MM, R. Blackburn
ATTN: MMETH, F. Walter
ATTN: MMEDD, C. Graham
ATTN: MMGRW, G. Fry
ATTN: MMIFM, S. Mallory
ATTN: MMETH, R. Padfield
ATTN: MMIFM, D. Stanger

DEPARTMENT OF THE AIR FORCE (Continued)

Ballistic Missile Office
Air Force Systems Command
ATTN: MNNL, S. Kennedy
ATTN: MNNH, J. Tucker
ATTN: MNNG

Foreign Technology Division
Air Force Systems Command
ATTN: TQTD, B. Ballard
ATTN: PDJV

Headquarters Space Division
Air Force Systems Command
ATTN: C. Kelly

Headquarters Space Division
Air Force Systems Command
ATTN: AQT, W. Blakney
ATTN: AQM

Headquarters
Electronic Systems Division
Air Force Systems Command
ATTN: Technical Library

Headquarters Space Division
Air Force Systems Command
ATTN: DYS, L. Darda

Headquarters Space Division
Air Force Systems Command
ATTN: SZJ, R. Davis

Headquarters Space Division
Air Force Systems Command
ATTN: SKF, P. Stadler

Rome Air Development Center
Air Force Systems Command
ATTN: RBRP, C. Lane
ATTN: RBRM, J. Brauer

Rome Air Development Center
Air Force Systems Command
ATTN: ETS, R. Dolan
ATTN: ESR, W. Shedd
ATTN: ESR, P. Vail
ATTN: ESE, A. Kahan
ATTN: ESER, R. Buchanan

DEPARTMENT OF ENERGY

Department of Energy
Albuquerque Operations Office
ATTN: Document Control for WSSB.

Department of Energy
ATTN: OMA

OTHER GOVERNMENT AGENCIES

Central Intelligence Agency
ATTN: OSI/RD

NASA
Goddard Space Flight Center
ATTN: J. Adolphsen
ATTN: V. Danchenko

OTHER GOVERNMENT AGENCIES (Continued)

Department of Commerce
National Bureau of Standards
ATTN: Security Officer for K. Galloway
ATTN: Security Officer for J. Humphreys
ATTN: Security Officer for J. Mayo-Wells
ATTN: Security Officer for J. French
ATTN: Security Officer for R. Scace
ATTN: Security Officer for S. Chappell
ATTN: Security Officer for W. Bullis

NASA
George C. Marshall Space Flight Center
ATTN: L. Haniter
ATTN: H. Yearwood
ATTN: EG02
ATTN: M. Nowakowski

NASA
ATTN: J. Murphy

NASA
Lewis Research Center
ATTN: M. Baddour

NASA
Ames Research Center
ATTN: G. DeYoung

DEPARTMENT OF ENERGY CONTRACTORS

Lawrence Livermore Laboratory
ATTN: Document Control for Technical Information Dept.

Los Alamos Scientific Laboratory
ATTN: Document Control for J. Freed

Sandia Laboratories
ATTN: Document Control for W. Dawes
ATTN: Document Control for R. Gregory
ATTN: Document Control for J. Hood
ATTN: Document Control for J. Barnum
ATTN: Document Control for F. Coppage

DEPARTMENT OF DEFENSE CONTRACTORS

Advanced Microdevices, Inc.
ATTN: J. Schlageter

Advanced Research & Applications Corp.
ATTN: R. Armistead

Aerojet Electro-Systems Co.
ATTN: T. Hanscome

Aerospace Corp.
ATTN: D. Fresh
ATTN: W. Willis
ATTN: S. Bower

Aerospace Industries Assoc. of America, Inc.
ATTN: S. Siegel

Battelle Memorial Institute
ATTN: R. Thatcher

BDM Corp.
ATTN: D. Alexander
ATTN: D. Wunch

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Bendix Corp.
Navigation and Control Group
ATTN: E. Meeder

Boeing Co.
ATTN: D. Egelkrout

Boeing Co.
ATTN: I. Arimura
ATTN: C. Rosenberg
ATTN: W. Rumpza
ATTN: A. Johnston
ATTN: C. Lancaster
ATTN: C. Dixon

Burr-Brown Research Corp.
ATTN: H. Smith

California Institute of Technology
Jet Propulsion Lab
ATTN: A. Shumka
ATTN: W. Price

Charles Stark Draper Lab, Inc.
ATTN: A. Schutz
ATTN: P. Greiff
ATTN: R. Bedingfield
ATTN: C. Lai
ATTN: R. Ledger

Cincinnati Electronics Corp.
ATTN: L. Hammond
ATTN: C. Stump

Control Data Corp.
ATTN: J. Meehan

University of Denver
Colorado Seminary
Denver Research Institute
ATTN: Security Officer for F. Venditti

E-Systems, Inc.
ATTN: K. Reis

Electronic Industries Association
ATTN: J. Hessman

EMM Corp.
ATTN: F. Krch

Exp. & Math. Physics Consultants
ATTN: T. Jordan

Fairchild Camera and Instrument Corp.
ATTN: R. Marshall
ATTN: Sec. Con. for D. Myers

Ford Aerospace & Communications Corp.
ATTN: J. Davison
ATTN: Technical Information Services

Ford Aerospace & Communications Corp.
ATTN: D. Cadle

Franklin Institute
ATTN: R. Thompson

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Garrett Corp.
ATTN: R. Weir

General Dynamics Corp.
ATTN: W. Hansen
ATTN: N. Cohn

General Dynamics Corp.
ATTN: R. Fields
ATTN: O. Woods

General Electric Co.
Space Division
ATTN: J. Peden
ATTN: L. Sivo
ATTN: R. Casey
ATTN: D. Long

General Electric Co.
Re-Entry & Environmental Systems Div.
ATTN: Technical Library
ATTN: J. Palchefsky, Jr.
ATTN: R. Benedict

General Electric Co.
ATTN: J. Reidl

General Electric Co.
Aircraft Engine Business Group
ATTN: R. Hellen

General Electric Co.
Aerospace Electronics Systems
ATTN: D. Cole
ATTN: J. Gibson
ATTN: W. Patterson

General Electric Co.
ATTN: D. Pepin

General Electric Company-TEMPO
ATTN: M. Espig
ATTN: DASIAC

General Electric Company-TEMPO
ATTN: W. Alfonte

General Research Corp.
ATTN: Technical Information Office
ATTN: R. Hill

George C. Messenger
Consulting Engineer
ATTN: G. Messenger

Georgia Institute of Technology
Georgia Tech. Research Institute
ATTN: R. Curry

Goodyear Aerospace Corp.
ATTN: Security Control Station

Grumman Aerospace Corp.
ATTN: J. Rogers

GTE Sylvania, Inc.
Electronics Systems Group-Eastern Div.
ATTN: C. Thornhill
ATTN: L. Pauples

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

GTE Sylvania, Inc.
ATTN: P. Frederickson
ATTN: H & V Group
ATTN: H. Ullman
ATTN: J. Waldron
ATTN: C. Ramsbottom

Harris Corp.
Harris Semiconductor Division
ATTN: C. Anderson
ATTN: J. Cornell

Honeywell, Inc.
Avionics Division
ATTN: R. Gumm

Honeywell, Inc.
Avionics Division
ATTN: C. Cerulli

Honeywell, Inc.
Radiation Center
ATTN: Technical Library

Honeywell, Inc.
Defense Systems Division
ATTN: K. Gaspard

Hughes Aircraft Co.
ATTN: J. Singletary
ATTN: R. McGowan

Hughes Aircraft Co.
ATTN: E. Smith
ATTN: W. Scott

IBM Corp.
ATTN: T. Martin
ATTN: H. Mathers
ATTN: F. Tietse

IIT Research Institute
ATTN: I. Mindel

Institute for Defense Analyses
ATTN: Tech. Info. Services

Intel Corp.
ATTN: M. Jordan

International Business Machine Corp.
Thomas Watson Research Center
ATTN: J. Ziegler

International Tel. & Telegraph Corp.
ATTN: A. Richardson
ATTN: Dept. 608

Intersil Inc.
ATTN: D. MacDonald

IRT Corp.
ATTN: J. Harrity

JAYCOR
ATTN: L. Scott

Kaman Sciences Corp.
ATTN: J. Lubell

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Johns Hopkins University
Applied Physics Lab
ATTN: P. Partridge

Litton Systems, Inc.
Guidance & Control Systems Division
ATTN: J. Retzler
ATTN: G. Maddox

Lockheed Missiles & Space Co., Inc.
ATTN: J. Smith
ATTN: J. Crowley

Lockheed Missiles & Space Co., Inc.
ATTN: E. Smith
ATTN: P. Bene
ATTN: C. Thompson
ATTN: H. Phillips

M.I.T. Lincoln Lab
ATTN: P. McKenzie
ATTN: Library A-082

Martin Marietta Corp.
ATTN: R. Gaynor
ATTN: H. Cates
ATTN: W. Brockett
ATTN: W. Janocko

Martin Marietta Corp.
ATTN: E. Carter

McDonnell Douglas Corp.
ATTN: Library
ATTN: M. Stich
ATTN: D. Dohm
ATTN: B. Kloster

McDonnell Douglas Corp.
ATTN: J. Holmgrem
ATTN: D. Fitzgerald

McDonnell Douglas Corp.
ATTN: Technical Library

Mission Research Corp.
ATTN: C. Longmire

Mission Research Corp.
EM Systems Applications Division
ATTN: R. Pease

Mission Research Corp.
ATTN: J. Azarewicz
ATTN: V. Van Lint
ATTN: J. Raymond
ATTN: R. Berger

Mitre Corp.
ATTN: M. Fitzgerald

Motorola, Inc.
Government Electronics Division
ATTN: A. Christensen

Motorola, Inc.
Semiconductor Group
ATTN: L. Clark

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

National Semiconductor Corp.
ATTN: A. London
ATTN: R. Wang

University of New Mexico
Electrical Engineering & Computer Science Dept.
ATTN: H. Southward

Northrop Corp.
Northrop Research & Technology Ctr.
ATTN: J. Srour
ATTN: T. Jackson
ATTN: P. Eisenberg

Northrop Corp.
Electronic Division
ATTN: L. Apodaca
ATTN: D. Strobel
ATTN: P. Gardner

Physics International Co.
ATTN: J. Shea
ATTN: Division 6000
ATTN: J. Huntington

R & D Associates
ATTN: R. Poll
ATTN: C. MacDonald
ATTN: S. Rogers

Rand Corp.
ATTN: C. Crain

Raytheon Co.
ATTN: J. Ciccio

Raytheon Co.
ATTN: A. Van Doren
ATTN: H. Flescher

RCA Corp.
Government Systems Division
Astro Electronics
ATTN: V. Mancino
ATTN: G. Brucker

RCA Corp.
David Sarnoff Research Center
ATTN: D. O'Connor
ATTN: Office N103

RCA Corp.
Government Systems Division
Missile & Surface Radar
ATTN: R Killion

RCA Corp.
ATTN: E. Van Keuren

RCA Corp.
Somerville Plant, Solid State Div.
ATTN: W. Allen

Rensselaer Polytechnic Institute
ATTN: R. Gutmann

Research Triangle Institute
ATTN: Security Officer for M. Simons, Jr.

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Rockwell International Corp.
ATTN: V. Strahan
ATTN: V. De Martino
ATTN: T. Oki
ATTN: J. Bell

Rockwell International Corp.
ATTN: D. Stevens

Rockwell International Corp.
ATTN: TIC BA08
ATTN: T. Yates

Sanders Associates, Inc.
ATTN: L. Brodeur

Science Applications, Inc.
ATTN: V. Verbinski
ATTN: J. Naber
ATTN: V. Ophan

Science Applications, Inc.
ATTN: W. Chadsey

Science Applications, Inc.
ATTN: D. Stribling

Singer Co.
ATTN: J. Brinkman

Singer Co.
ATTN: R. Spiegel

Sperry Rand Corp.
Sperry Microwave Electronics
ATTN: Engineering Laboratory

Sperry Rand Corp.
Sperry Division
ATTN: P. Maraffino
ATTN: C. Craig
ATTN: F. Scaravaglione
ATTN: R. Viola

Sperry Rand Corp.
Sperry Flight Systems
ATTN: D. Schow

Sperry Univac
ATTN: J. Inda

Spire Corp.
ATTN: R. Little

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

SRI International
ATTN: A. Whitson
ATTN: P. Dolan

Teledyne Ryan Aeronautical
ATTN: J. Rawlings

Texas Instruments, Inc.
ATTN: R. Stehlin
ATTN: A. Peletier

TRW Defense & Space Sys. Group
ATTN: A. Pavelko
ATTN: P. Guilfoyle
ATTN: A. Witteles
ATTN: R. Kingsland
ATTN: H. Holloway
ATTN: O. Adams
ATTN: R. Schnieder
ATTN: H. Haid

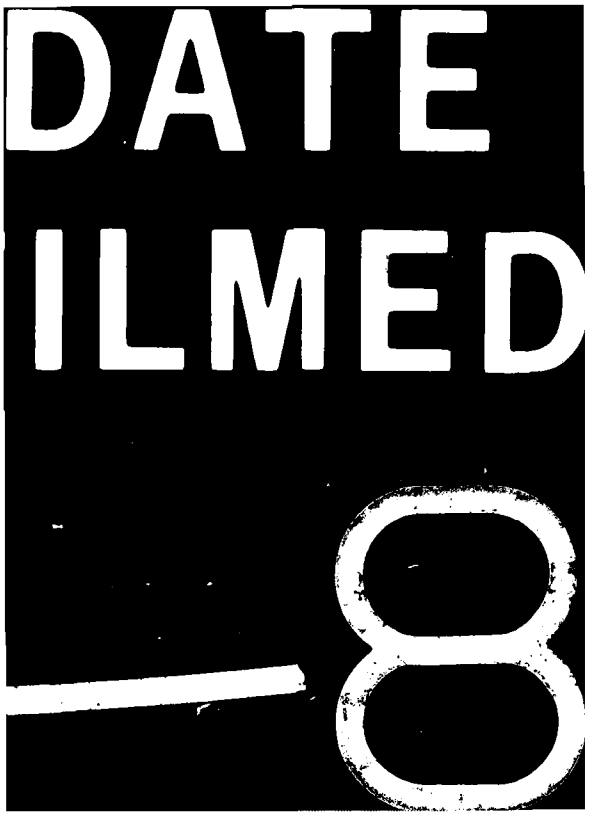
TRW Defense & Space Sys. Group
ATTN: R. Kitter
ATTN: F. Fay
ATTN: M. Gorman

TRW Systems and Energy
ATTN: D. Millward
ATTN: G. Spehar

Vought Corp.
ATTN: Technical Data Center
ATTN: R. Tomme
ATTN: Library

Westinghouse Electric Co.
Aerospace & Electronic Systems Div.
ATTN: L. McPherson

Westinghouse Electric Corp.
Defense and Electronic Systems Ctr.
ATTN: H. Kalapaca
ATTN: D. Crichi


DATE
ILMED
8